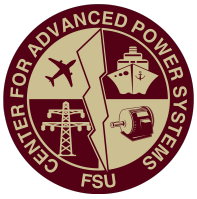


Cell Controller Design and Evaluation for a Switched-Capacitor Modular Multilevel Converter

submitted as a Research Report for the Austrian Marshall Plan Foundation

by

Matthias Musil BSc

September 2020

Project supervisors

Dr. Fang Z. Peng
Dr. Peter Zeller

Additional advisors

Dr. Yanjun Shi
Gernot Trauner MSc

Acknowledgements

I'd like to thank Dr. Fang Peng for officially supervising this project on the FSU side. His expertise in the field of power electronics and electronics in general definitely helped shaping this work and his style of teaching and giving feedback helped me getting a deeper understanding of what I'm doing. I'm looking forward to continue working with Dr. Peng in the future.

I also want to thank Dr. Peter Zeller for initiating the cooperation between the FH Wels and FSU which laid out the groundwork for this project. Furthermore I want to thank him for his continued guidance throughout my time in the Electrical Engineering master's program at the FH Wels and on this, and all other works I've conducted during my studies.

Then I'd also like to thank Dr. Michael 'Mischa' Steurer for giving me the opportunity to work on this project, which will eventually be turned into my Master's thesis, at the Center for Advanced Power Systems. Also I want to thank him for all his support and guidance throughout the course of the project.

Next, I want to thank Dr. Yanjun Shi for his unofficial supervision of this project on the FSU side. His feedback and our discussions from countless meetings were very valuable for the progress of this work. Dr. Shi often managed to ask in a way which made me question what I've been doing and in turn helped me improve my circuit and PCB designs.

Furthermore, I sincerely have to thank Gernot Trauner for unofficially supervising this work on the FH Wels side. He was always available when I had specific questions and definitely contributed to the success of this work. Mr. Trauner also supervised my Bachelor's thesis and we've since continuously had a very good cooperation, which we can hopefully keep up.

Of course I also have to thank Christoph Diendorfer and Christian Gruberbauer for their organizational support and the commitment to let me use space and equipment in the high voltage lab for the testing of the hardware designed in this project. Further, I wanted to mention that I highly appreciate our discussions during coffee breaks and the fact that working with them is always a joy.

Thanks also go to the International Office at the FH Wels which provided a great deal of support before and during this work. Thanks to them it was also possible to quickly change the mode of the project and return to Austria to continue working there.

I want to thank everybody who was also involved in or supported me during working on this project and has not been mentioned above.

Finally, I want to thank the Austrian Marshall Plan Foundation for granting me the Marshall Plan Scholarship which enabled me to conduct this research project at the Florida State University's Center for Advanced Power Systems.

Abstract

The goal of this project is to develop a cell controller for a switched capacitor modular multilevel converter which utilizes silicon carbide half bridge modules. It should transmit switching states from a main controller to the gate drivers, measure the cell capacitor's voltage and the heat sink's temperature and send that data back to the main controller. The cell controller is also responsible for the handling of fault signals and states. Since heavy electromagnetic interference (EMI) is expected, a strong emphasis lies on a robust design of both hardware and software. A circuit concept is proposed based on a literature review and then developed whilst considering intensive EMI mitigation strategies. A PCB design is created also under consideration of EMI mitigation strategies and common PCB design principles. The firmware for the cell controller is developed and tested successfully utilizing FPGA in the loop simulations. Since the PCB prototypes have not arrived at the time of writing this report, no measurements or hardware testing has been done yet. Work on the cell controller will continue though until a functioning device is achieved.

Contents

1 Introduction

1.1 Background and Motivation

The intention of this research project is to design and evaluate a cell controller for a switched-capacitor modular multilevel converter (SC-MMC) which is under development at the Center for Advanced Power Systems (CAPS). It is comprised of a modifiable number of switching cells, from at least 9 up to 30, in half bridge configurations to form a three phase inverter. The general circuit structure can be seen in Fig. 1.1. More precisely, 10 kV

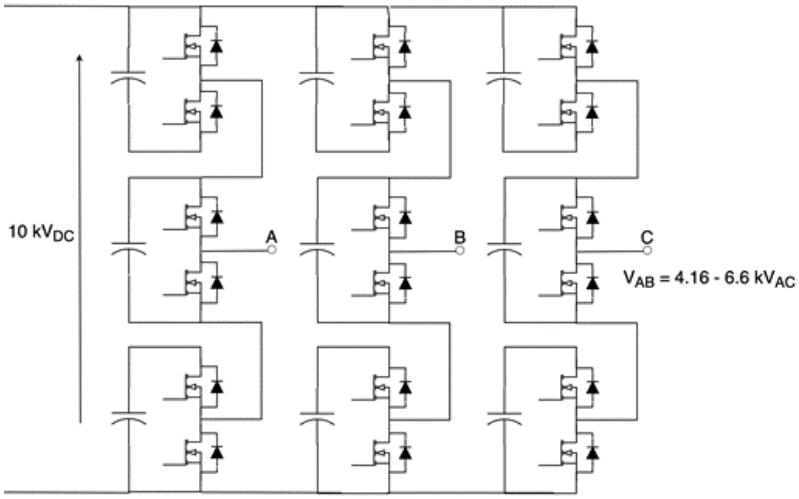


Figure 1.1: Circuit structure of the switched capacitor modular multilevel converter

half bridge SiC (silicon carbide) modules are connected in parallel with high voltage low ESL (equivalent series inductance) capacitors to form a switching cell, which is operated at around 5 kV.
Each of these cells requires a separate control board which receives commands from a main controller, which runs the control logic and supervises the operation of the SC-MMC. This cell controller sends firing pulses to the gate drivers at the semiconductor switches. It also needs to measure the cell capacitor voltage, the temperature at the heat sink, capture fault signals from the gate drivers and send this information to the main controller. Since the cell controller has to be placed directly on or very close to the SiC half bridge module, heavy electromagnetic interference is to be expected. If not handled carefully, this could not only disturb signals but even damage the controller IC itself and consequently lead to the faulty operation of or damage to the SC-MMC. Therefore a big focus of this project also lies on identifying and mitigating EMI arising from operating the controller board in the vicinity of the SiC module.

This SC-MMC is a novel power electronics application utilizing modern wide bandgap switching devices. Since these devices are considerably smaller compared to conventional

Si modules at comparable ratings, the cell controller boards and voltage sensors also need to be minimized in size. Additionally, the drastically increased switching speeds of SiC switches compared to traditional Si switches also gives rise to increased electromagnetic interference. Considerable effort will have to be expended into making the controller robust against influences by the harsh electromagnetic environment it should operate in. Since a large number of cell controllers will communicate with a main controller, an effective data transmission with minimum channels and latency needs to be developed.

The parent project is funded by the Advanced Manufacturing Office of the US Department of Energy and executed at the National Renewable Energy Laboratory (NREL) . With a combined funding of around 7 million dollars, NREL, FSU (Florida State University) and OSU (Ohio State University) will jointly build and demonstrate a 13.8 kV back to back converter using high voltage SiC MOSFET modules. One of the project goals is to investigate the effects of wide bandgap devices onto the power grid in the medium voltage megawatt scale. FSU's contribution to this project is to develop half of this converter, advance the medium voltage power hardware in the loop (PHIL) and controller hardware in the loop (CHIL) simulation capability, and to integrate and commission the converter in FSU's PHIL environment. Therefore, the outcome of the research work documented in this report will directly benefit the outcome of the overall research project.

1.2 Objectives

The general objectives of this project are to:

- Select a suitable control IC to handle the required tasks and generate gate signals, e.g. a digital signal processor (DSP), microcontroller, field programmable gate array (FPGA) or complex programmable logic array (CPLD)
- Implement the cell voltage and the heat sink temperature measurement with small footprint sensors and the required signal conditioning
- Develop a communication protocol to effectively transmit data via optical fibers between cell and main controller while reducing channels and latency
- Simulate and verify the cell controller circuit and functions in a FPGA-in-the-loop (FIL) simulation
- Determine EMI performance and issues by utilizing FEM simulation tools and compare performance of commercial, plugged controller cards or evaluation boards with that of the controller IC directly soldered onto the cell controller PCB
- Create a design which is robust against EMI (electromagnetic interference)
- Control power consumption, costs and footprint
- Implement a batch firmware update functionality to simplify and accelerate updating of a large number of cell controllers

- Test and evaluate the cell controller design against the mentioned requirements
- Derive possible improvements

1.3 Approach

The objectives of this project are achieved through multiple steps. The first one is to determine the specifications of a switching cell and thus the requirements for the cell controller. These include, among others, the cell voltage, temperature range, specifications of the SiC device and the switching frequency. Based on these requirements and a comparison of their quantitative and qualitative properties, a suitable type of controller IC, i.e. a DSP, CPLD, FPGA or microcontroller, and thus a development board is then selected for prototyping and development purposes.
A literature review is then conducted to determine possible EMI issues already at the early circuit development stage, in order to have them considered in every aspect of the design. This review focuses on EMI issues related to SiC devices and similar applications.
Based on the cell specifications and requirements, a voltage and temperature sensor circuit, the sensor board, is developed. Furthermore, the optical interfaces and further circuit components are determined.
Using an FPGA/Controller-in-the-loop simulation, the basic functionality of the controller firmware, including the communication protocol, will be implemented for testing but also the determination of logic and power requirements of the controller IC.
The power requirement estimation is then performed for all other components in order to design a suitable local power supply.
At this stage, a specific controller IC is selected for the final design. EMI considerations and controller requirements which are determined until then will flow into this decision.
The next step would have been to perform an EMI simulation and determine best practices for the design of the controller board. Due to time restrictions and knowledge gained by the literature review and insights provided by project partners no such simulations were carried out.
Now the sensor and cell controller PCBs, from here on called the sensor board and the controller board, will be designed, whilst considering the findings from the literature review and common EMC practice in PCB design. In parallel to the PCB design, a failure mode and effects analysis (FMEA) is performed as a substitute to EMI simulations. This analysis aides with the detection of possible failure modes, is thus a tool to further improve circuit & PCB designs and prevent these failures.
Eventually, work on the firmware will be continued and finalized, including a batch firmware updating function to quickly update all cell controllers at once.
Finally, if time allows, the PCB is manufactured, assembled and tested according to the required specifications and findings of the FMEA.
At the time of finishing this report, the PCB prototypes have not arrived from manufacturing and therefore could not be tested yet. Similarly, the FMEA is still ongoing. Work on

this project is going to be continued until the cell controller components have been tested successfully under all stated conditions.

1.4 Expected Outcome

The outcome of this research project is expected to be a fully functioning cell controller for the switched capacitor modular multilevel converter. The design and, if possible, testing procedures should give new insights into EMI compliant design in medium voltage converter systems utilizing wide bandgap devices and effective, noise immune communication between cell and main controllers of modular multilevel converters. As it contributes to the overall project, this project also plays a part in determining the effects of wide bandgap power electronic devices onto medium voltage grids.

1.5 Report structure

This report is thematically structured. After this introduction follow the specifications of the switching cell and the requirements for the cell controller and its components. The literature review of EMI aspects is summarized in the following chapter. Then the circuit design and implementation for the sensor and controller board circuits are presented. Following the circuit design, the PCB design for both boards is discussed. The firmware including the communication protocol is covered in the sixth chapter. Finally, a conclusion summarizes the work covered in this report and is followed by an outlook into the continuing work on this project.

2 Specifications and requirements

2.1 Switching cell components and operating specifications

The specifications of the switching cell were determined based on component data sheets and operational specifications of the SC-MMC design.

The switching cell is comprised of a half-bridge module and a DC-link capacitor. The half-bridge module is a 10 kV **CREE SiC Half-Bridge Module** which was received as an engineering sample about which no information may be disclosed as of yet.

The DC-link capacitor is a **Ducati DCH 86 P**:

- Rated capacitance $C_n = 120\ \mu F$
- Rated DC voltage $V_n = 6800$ V
- Equivalent series resistance ESR = 1.5 $m\Omega$ @ 1 kHz
- Equivalent series inductance ESL = 40 nH

For the operation of the switching cells and the SC-MMC, the following specifications were given by the responsibles:

- Nominal capacitor operating voltage = 4.8 kV $\pm 5\%$
- Maximum expected capacitor overvoltage = 6 kV
- Regular operational temperature range = 20 to 100 $°C$
- Nominal half-bridge module switching frequency $f_{sw} = 2$ kHz

2.2 Voltage and temperature sensor requirements

The following requirements are given for the voltage and temperature sensor:

- Minimum required voltage measurement resolution = 12 bit
- The voltage sensor sampling rate and bandwidth should be high enough to be able to measure the switching ripple of the cell voltage.
- The sensor should be galvanically isolated from the cell controller board and located as close as possible to the measured signal.
- The temperature sensor should measure the temperature of the electrically floating heat sink and thus also be galvanically isolated from it.
- The sensor board needs to create its own supply voltage from a 15 V supply at the low side gate driver and avoid the coupling of common mode (CM) noise into the measurement circuit. Around 1.2 W of power are available.
- Robustness should be prioritized over accuracy.

2.3 Controller requirements

Requirements for the controller are given by design criteria of the SC-MMC and the sensor:

- The controller should provide three switching states (10, 01, 00) based on information from the main controller, the shoot through state (11) needs to be prevented.
- For the gate signals mentioned above, the controller should be able to generate adjustable deadtimes, which in turn should be adjustable through the main controller.
- The controller should presume protection functions, such as blocking the switches immediately upon receiving a fault signal from a gate driver and indicating the fault to the main controller. It should also detect overvoltage (OV) or over temperature (OT) and act accordingly.
- The controller should constantly report the cell voltage and temperature to the main controller, and notify it about faults.
- All main controller communication should be implemented with one upstream and one downstream optical fiber using a custom communication protocol which should be implemented for very high EMI (electromagnetic interference) robustness.
- The controller should have a means of status indication which is visible in the assembled state. These statuses should be indicated: Power on, fibers plugged in, fault, OV/OT and main control IC running.
- Debugging functions are required for a smooth testing: Oscilloscope probe test points for major signals and a manual reset switch.
- Electromagnetic compatibility (EMC) is the most important design criteria. It should be considered in all design stages, in order for the circuit to remain normal operation in close vicinity (ca. 10 cm) of the SiC module. Common mode noise immunity, although provided by auxiliary power supply and gate driver, should be reinforced and space for EMI shielding should be reserved. The placement of the controller IC should consider the radiation loop from the main power circuit. Any noise applied on sensor and signal conditioning circuits should be mitigated either by hardware or software filters. This should also consider the startup time of the controller IC after an operational breakdown.
- A fast batch firmware updating method should be considered to be able to deploy firmware updates quickly and in-circuit to a total of 9 cells.
- The controller board should be galvanically isolated from every other component of the switching cell.
- It needs to create its own supply voltages from a 24 to 30 V auxiliary power supply. Around 6 W are available.

3 Literature review

3.1 Introduction

This literature review focuses specifically on the EMI aspects of SiC or wide bandgap devices in general, since these novel devices employ significantly faster switching speeds than their well-known conventional Si counterparts and thus bring new challenges, among which EMI is one of the major concerns. The EMI behavior of and countermeasures for Si devices have already been well studied and documented in the past, while there are still many new discoveries being made for wide bandgap devices.
This review will start with a short explanation of the types of EMI, followed by the special properties of wide bandgap devices. Then some EMI aspects and discoveries from various papers will be summarized and possible mitigation strategies will be discussed.
Most of the review is done based on the review paper [1] as it very recently gathered and summarized a great portion of the EMI research on wide bandgap devices.

3.2 Types of EMI

In the English language, electromagnetic interference (EMI) and noise are usually used to describe the same phenomena acting on and disturbing electrical circuits. Especially in literature they are used distinctively to describe certain properties of a disturbance though. The term EMI is used when classifying the propagation mode of noise. Generally, there is conducted and radiated EMI. The term noise is used to describe the different modes of conducted EMI. There is differential mode (DM) and common mode (CM) noise. These four terms will be shortly explained in the following.

3.2.1 Conducted and radiated EMI

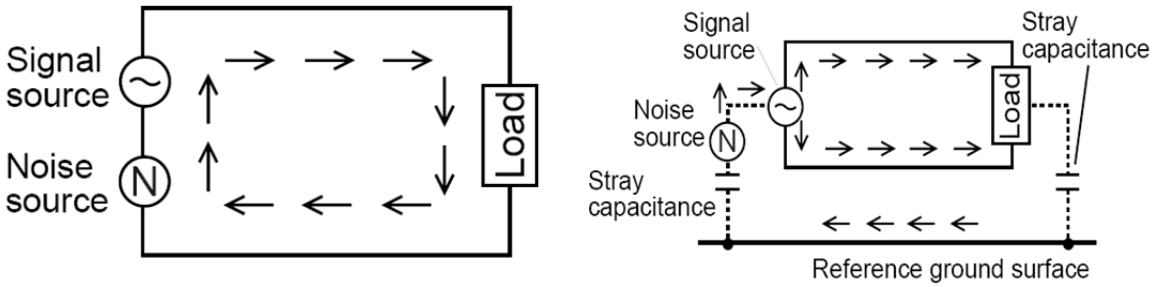
Conducted EMI is noise which is generated by a subcircuit and transferred to another subcircuit through a conductive path, like cables, PCB traces, GND planes or even parasitic capacitors. Switching devices like SiC MOSFETs in switching converters are common sources of conducted EMI which might then be conducted to the load, to the supply feeding the converter, but also to the measurement and control circuits. Conducted EMI is usually classified in the frequency range from around 150 kHz to 30 MHz. [1] As will be shown in section 3.4, switching speed and frequency are dominant in this frequency range, therefore it can be said that conducted EMI is mostly determined by these two parameters. Since this form of EMI is conducted, it is also strongly influenced by the impedance of the EMI propagation path, which in turn depends on the circuit topology, grounding connections and component characteristics. [1]

Radiated EMI is noise which travels through air, i.e. when a circuit is disturbed by another circuit operating somewhere in the distance with no direct wired connection. Usually radiated EMI is classified at above 30 MHz and described by far field coupling. [1] There is also a near field coupling though which does not quite fulfill the definition of radiated EMI but still transfers noise through air.
Near field coupling occurs at distances $r < \frac{\lambda}{2\pi}$ where λ is the wavelength of the signal. Here, the electric (E) and magnetic (H) field are decoupled from each other and are determined by voltage, current and geometry of the noise source. Usually one of the two fields will be dominant. E field coupling occurs across parasitic capacitances. Typical sources of E field coupling are pulsating voltages. H field coupling is determined by mutual inductances and thus depends on current loops. [1]
Far field coupling occurs at distances $r >> \frac{\lambda}{2\pi}$. In this region the E and H fields are coupled via Maxwell's equation and the noise is transferred via electromagnetic waves. Generally, any conductor or loop can act as an antenna for sending or receiving noise and either is strongly influenced by geometry. [1]

3.2.2 Differential and common mode noise

As mentioned before, DM and CM noise are forms of conducted EMI. Both are illustrated in Fig. 3.1. DM noise is conducted on two lines in the opposite direction to each other, which is usually also the conduction mode of the wanted signal. The noise source appears across the signal lines and in series with the signal source. Since it circulates in the circuit, the DM noise path and severity is determined by circuit topology and component characteristics [1].

CM noise is conducted in the same direction on all lines. The noise source couples a noise current via stray capacitances into the circuit from where it couples to the reference ground and back to the noise source. Also, it was shown in [2] that the major contributor for CM noise in single phase converters is the parasitic capacitance.



(a) Differential mode noise (b) Common mode noise

Figure 3.1: Equivalent circuits for different kinds of noise [3]

Now although these two types of noise are conducted EMI, they also contribute to the generation of radiated EMI. Generally, CM noise can produce stronger radiated EMI

because the affected signal and ground lines often form large loop areas. Since DM noise currents flow in opposite directions, their fields may cancel and thus produce less radiation.

3.3 Wide bandgap devices

Wide bandgap (WBG) materials such as silicon carbide (SiC) or gallium nitride (GaN) have significantly improved properties compared to conventional silicon (Si). They employ a higher critical electrical field strength, a higher saturation drift velocity and better thermal conductivity [1]. For these reasons, WBG devices can be created with much smaller die sizes at the same voltage rating as Si devices. This leads to a smaller junction and junction capacitance, which can be down to a 10^{th} of Si dies. Since a MOSFETs switching speed is determined by this capacitance and the gate resistor, significantly faster switching speeds can be achieved. A comparison of device capacitances is given [1] and a comparison of the switching speeds of an Si MOSFET and a GaN HEMT (high electron mobility transistor) was done in [4]. Fig. 3.2 shows the switching waveforms presented in that paper. It can be seen that the wide bandgap device switches considerably faster than the conventional Si MOSFET. The increased switching speed also leads to reduced

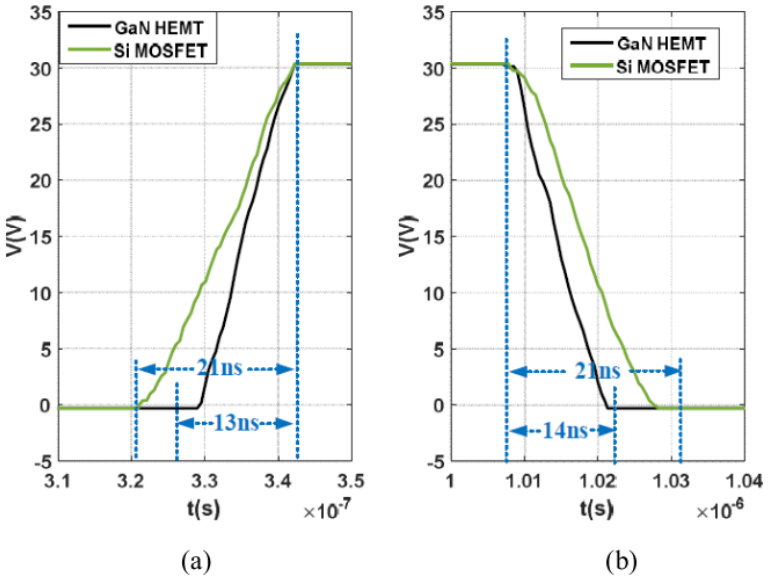


Figure 3.2: Switching waveform comparison GaN HEMT vs. Si MOSFET during (a) turn-off and (b) turn-on [4]

switching power losses and thus allows for higher operating frequencies, which in turn enables higher efficiency and higher power density designs.
In conclusion, WBG devices are advantageous for high efficiency and high power density designs, but, from an EMI perspective, will lead to issues with conductive and radiated EMI. [1]

3.4 EMI aspects of WBG devices and research findings

The previous section highlighted the advantages and positive aspects of WBG devices. However, faster switching and higher operating frequencies are not just advantageous. Increased voltage and current rise times, $\frac{dv}{dt}$ and $\frac{di}{dt}$, lead to HF voltage and current ringing during switching transients. The oscillation frequency, according to [5], can be expressed by

$$f_{osc} = \frac{1}{2\pi\sqrt{L_p C_j}} \tag{3.1}$$

where L_p is the parasitic inductance of the layout and C_j is the device's junction capacitance. Taking a typical L_p of around 50 nH and the C_j of an SCT20N120 SiC MOSFET (1200V, 20A), which is 650 pF, an oscillation frequency of 27.2 MHz is predicted. Taking the IXFX20N120, which is a comparable Si MOSFET with the same ratings and a C_j of 7400 pF, the oscillation frequency is only 8.27 MHz. According to [4], the oscillation frequency in WBG applications can go into the hundreds of megahertz. The HF ringing caused by WBG devices is therefore significantly more severe and difficult to reduce, because EMI filters have limited performance at HF due to the used magnetic materials and their parasitic parameters.

A simulation case study was done in [1] to show the impact of switching speed, operating frequency and voltage ringing on the EMI spectrum of a WBG device in a buck converter circuit. The resulting EMI spectra are shown in Fig. 3.3. The three cases are:

1. Switching frequency f_{sw1} and switching speed represented by turn on/off times t_{r1} and t_{f1}
2. Same switching frequency f_{sw1}, higher switching speed: $t_{r2} < t_{r1}$ and $t_{f2} < t_{f1}$
3. Higher switching frequency $f_{sw2} > f_{sw1}$, same switching speed as in case 2, voltage ringing is included

The duty cycle is 0.4 for all cases.

On an initial note, the radiated EMI range was drawn a decade to far in the figure. It should start at 30 MHz, which is indicated by the red line.
By comparing case 1 and 3, it can be seen that the low frequency EMI is determined by the switching frequency and magnitude of the switching waveform. According to [6], the roll-off corner frequency f_c is determined by either the turn-on or turn-off time, whichever is smaller. This is confirmed by comparing cases 1 and 2. At the same switching frequency but different switching speeds, the roll-off frequency in case 2 is higher than in case 1. From $t_{r2} < t_{r1}$ and $t_{f2} < t_{f1}$ follows $f_{c2} > f_{c1}$. As a result, the total noise spectrum is higher in case 2, i.e. the EMI is more severe. Furthermore, the voltage ringing in case 3 causes a spike in the EMI spectrum at the resonant frequency f_{res}, which refers to the oscillation frequency f_{osc} from the discussion of HF voltage ringing earlier in this section. It can be concluded, that the HF EMI is determined by the switching speed and voltage ringing. It

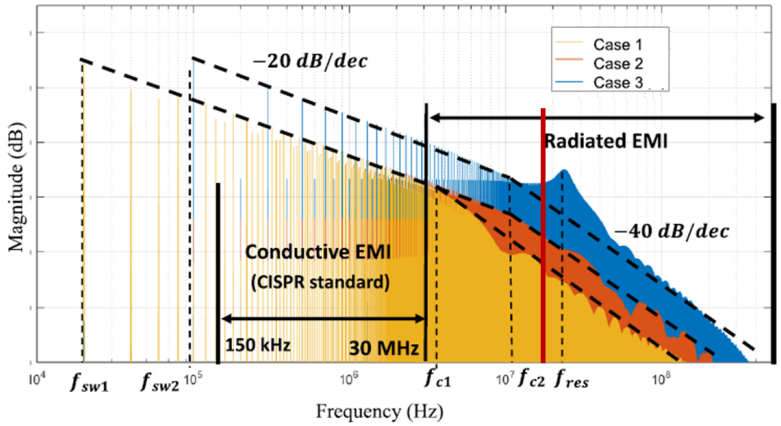


Figure 3.3: Frequency spectra of the drain-source voltage of a PWM buck converter for different cases [1]

can also be noted, that an increase of the switching frequency causes an overall increase of the EMI.
This case study clearly shows the EMI issues which arise from increased switching frequencies and switching speeds in applications with WBG devices.

A comparison of the conducted EMI of Si IGBTs and SiC MOSFETs in a matrix converter was done in [7]. Both switch at the same frequency of 10 kHz, the SiC MOSFET's switching speed is 11 $kV/\mu s$ and the Si IGBT's is 6.6 $kV/\mu s$. The measured current spectra in Fig. 3.4 show that the LF EMI is comparable, which fits with the previously made statement that this EMI region is dominated by the switching frequency. At the HF range above 10 MHz however, the measured EMI of the SiC MOSFET is around 20 dB higher than the Si IGBT's. This confirms the statement, that the HF EMI range is dominated by the switching speed. Furthermore, also also stated before, noise in this frequency range is significantly more difficult to filter.

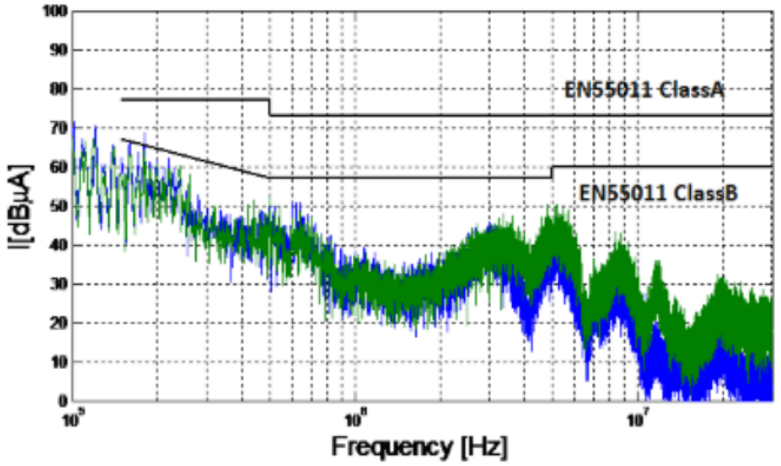


Figure 3.4: Measured conducted EMI for Si IGBT (blue) and SiC MOSFET (green) [7]

Another evaluation of the conducted EMI in a WBG application is given in [8], where

a 1 kW, 400 V inverter is operated at different switching frequencies, once with GaN HEMT switches and once with SiC MOSFETS. The inverter circuit including parasitic capacitances and expected CM current propagation paths is given in Fig. 3.5. Fig. 3.6 shows the input and output CM current spectra in the conducted EMI frequency range up to 30 MHz for the inverter operating with GaN HEMTs and Fig. 3.7 shows the spectra for the inverter operating with SiC MOSFETs. The spectra for the inverter operating

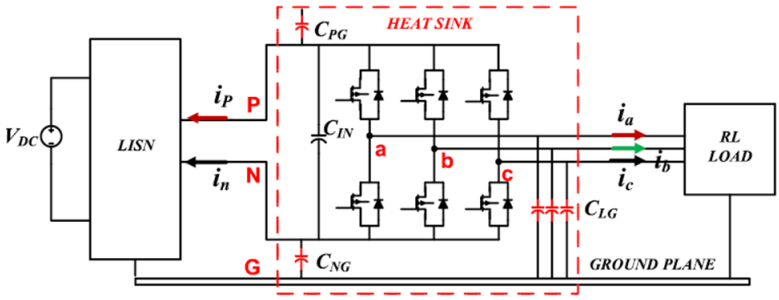


Figure 3.5: Three phase inverter with parasitic capacitances [8]

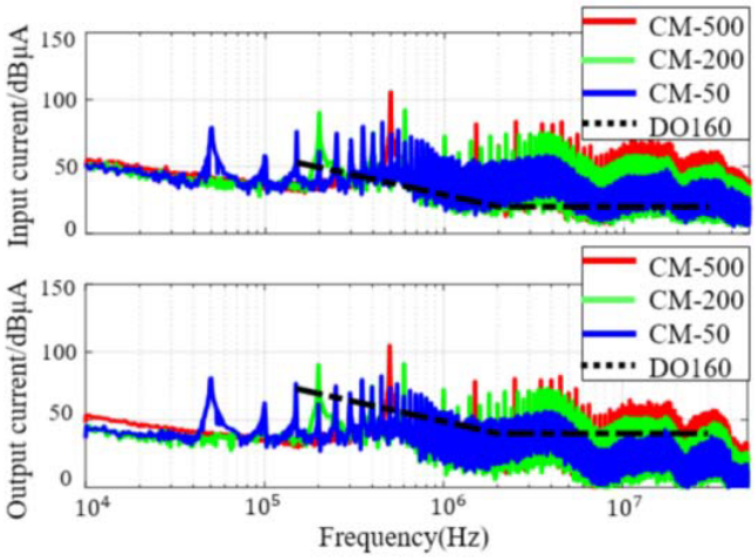


Figure 3.6: Input and output CM current spectra in the conducted EMI range for a GaN HEMT inverter at different switching frequencies (in kHz) [8]

with either WBG device shows again the influence of the switching frequency on the conducted EMI. In the GaN HEMT inverter, the conducted EMI is increased by 20 dB when increasing the switching frequency from 50 to 500 kHz. At the SiC MOSFET inverter an almost 20 dB increase of the EMI is already observed at an increase of the switching frequency from 20 to 70 kHz. This can be explained by the fact that GaN devices exhibit even smaller parasitic capacitances than SiC devices. The DO160 curve in Fig. 3.6 is an EMI standard which has to be fulfilled by electronics in airborne equipment. It can be seen that the output current spectrum at 50 kHz barely fits into the standard, while all higher

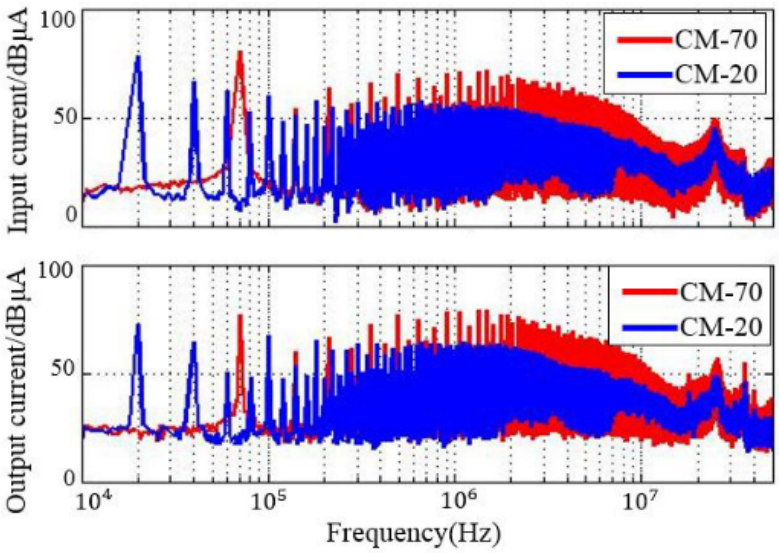


Figure 3.7: Input and output CM current spectra in the conducted EMI range for a SiC MOSFET inverter at different switching frequencies (in kHz) [8]

switching frequencies clearly fail the requirement of the standard. Similarly, although the curve is not drawn in Fig. 3.7, the SiC converter fails the standard's requirements in both measured cases. This again highlights the EMI issues present at WBG devices and shows how important a careful and sophisticated EMI compliant design is for applications utilizing WBG devices.

A comparison of the radiated EMI generated by converters with Si MOSFETs and GaN HEMTs was done in [4]. A dual active bridge converter was operated in a semi-anechoic chamber where the radiated EMI was measured with an antenna at a distance of 3 m. Fig. 3.8 shows the spectra of the switching voltage waveforms in the radiated EMI

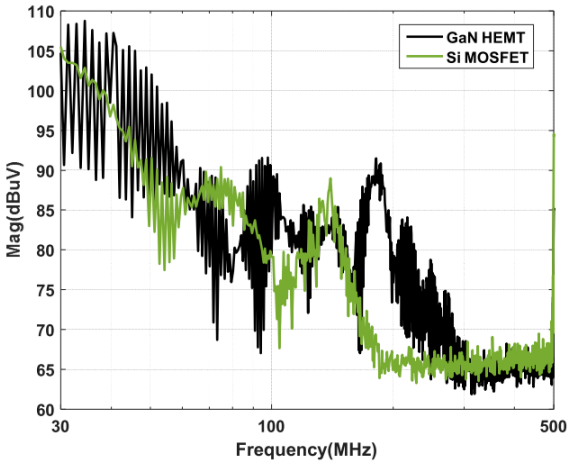


Figure 3.8: Spectra of the voltage across the semiconductor switches [4]

frequency range from 30 to 500 MHz. It can be seen that the GaN HEMT's spectrum is considerably more severe in the 30 to 60 MHz range. Also, there is a large HF peak at

around 180 MHz where the Si MOSFET's spectrum is already very low. The spectra of the

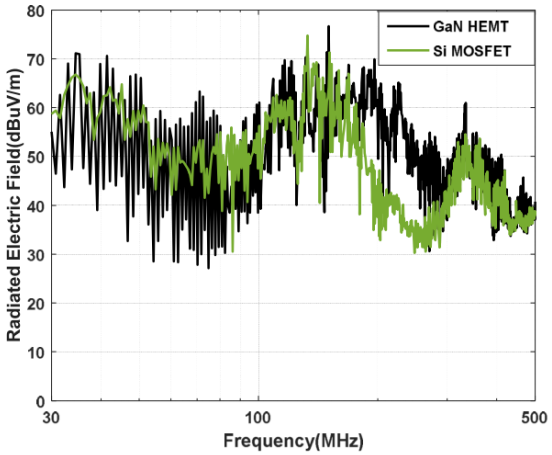


Figure 3.9: Spectra of the radiated electric fields of the converters with Si MOSFETs and GaN HEMTs [4]

radiated electric fields which were received by the antenna show that the GaN HEMT's radiated EMI noise is around 25 dB higher than that of the Si MOSFET in the range from around 180, where the large peak is visible in the switching waveform spectrum, to 300 MHz.
It was already determined, that the EMI spectrum of WBG devices is higher than that of Si devices. Since the impedance of parasitic capacitances reduces with an increase of the frequency, the noise of WBG devices will propagate through these paths with reduced impedance. The unintentional antenna caused by the circuit and parasitic capacitances therefore experiences a high current flow which leads to increased radiated EMI noise. [1] This was shown in the findings above.

Further comparisons between Si and WBG device applications are given in [9] and [10]. The findings summarized in this section lead to the conclusion, that a more careful design of the main power circuit comprised of WBG devices and more sophisticated EMI measures around the main power circuit and all adjacent circuits are necessary in order to achieve a reliable design utilizing WBG devices when compared to conventional Si applications.

3.5 EMI mitigation strategies

EMI can be mitigated either directly at the source or at the receiver. Since the cell controller developed in this project is an EMI receiver and its design has no influence on the SiC HB module's performance as a noise source, this review focuses on mitigation strategies at the receiving side. For completeness, a short summary of possible EMI reduction techniques at the source, from [1] and [11], is given here:

- Slow down the switching process to reduce HF noise, e.g. with gate resistors
- Reduce switching frequency to reduce LF noise

- Develop an active gate driver (AGD), e.g. as proposed in [12] where the gate resistance is adjusted to the current phase of the switching operation
- Damping ringing and voltage rise/fall times with RC snubbers or ferrite beads
- Minimize parasitic inductance in current commutation loops
- Reduce parasitic capacitances, e.g. to heat sink which is a big contributer to CM noise [13]
- Gate signal modulation techniques

Further considerations about reducing EMI emissions are discussed in [14]. This app note, although published in 1996, contains a lot of valuable information about EMI in microcontroller applications, which is still valid today and also applies to FPGA designs, which is why the following discussion will be based on this document, with some examples added for clarity. Fig. 3.10 gives a summary of different EMI propagation paths and how to reduce EMI along these paths. When discussing EMI mitigation techniques, a distinction

Problem	Solution See (b)
Radiated Field to Interconnecting Cable (Common-Mode)	2, 7, 8, 9, 11
Radiated Field to Interconnecting Cable (Differential-Mode)	2, 5, 6
Interconnecting Cable to Radiated Field (Common-Mode)	1, 3, 9, 11
Interconnecting Cable to Radiated Field (Differential-Mode)	1, 3, 5, 6, 7
Cable-to-Cable Crosstalk	1, 2, 3, 4, 5, 6, 10, 11
Radiated Field to Box	12, 13
Box to Radiated Field	12, 13
Box-to-Box Radiation	12, 13
Box-to-Box Conduction	1, 2, 7, 8, 9
Power Mains to Box Conduction	4, 11
Box to Power Mains Conduction	4, 11
Electromagnetic Interference Coupling Paths	4

(a) EMI propagation paths

Solution	Complexity	Cost
1. Insert Filter in Signal Source	Low	Medium
2. Insert Filter in Signal Receptor	Low	Medium
3. Insert Filter in Power Source	Low	Medium
4. Insert Filter in Power Receptor	Low	Medium
5. Twist Wire Pair	Low	Low
6. Shield Cable	Low	Medium
7. Use Balanced Circuits	Medium	Medium
8. Install Differential Line Drivers and Receivers	Medium	Medium
9. Float Printed Circuit Board(s)	Medium	Medium
10. Separate Wire Pair	Low	Medium
11. Use Ferrite Beads	Low	Medium
12. Use a Multilayer Instead of a Single Layer Printed Circuit Board(s)	Medium	High

(b) EMI fixes

Figure 3.10: A summary of EMI propagation paths and fixes [14]

is made between intra-system EMI and inter-system EMI. Inter-system EMI refers to interference between two or more independent circuits or systems, like from the SiC HB module to the cell controller circuit. Usually EMI enters or exits via antennas, therefore inter-system EMI is mostly a radiated or coupled EMI problem. Intra-system EMI problems distinguishes itself to inter-system EMI by the fact, that only the specimen (circuit, device) of concern is considered. The primary emphasis here is on considerations about

self-jamming, susceptibility to outside conducted or radiated noise or its own undesired emissions. [14]

The main EMI control techniques for intra-system EMI are shielding, filtering and wiring. [14]
Shielding reduces the radiated EMI received by a victim circuit. Shields are usually made of metal or ferrites and are placed around the victim circuit with as little gaps or holes as possible. The shield type needs to be carefully selected for the expected frequency range of noise. Metal shields (conductive shielding) are more suitable for medium to high frequency noise while ferrite shields (magnetic shielding) are more suitable for DC to low/medium frequency noise.
Filters are used to reduce or eliminate conducted EMI. They are placed at the source, receiver or both. A distinction is made between CM and DM noise filters. In many applications, a combination of both is favorable. Filters don't just have to be implemented in hardware. Thanks to powerful signal processors and FPGAs, anti-EMI filters can also be designed digitally as is shown in [15].
Wiring is required to connect different circuits together to form a system and have a great influence on both its EMI susceptibility and emission. Cables basically form antennas which can send and receive noise and proper wiring is therefore a critical component of an EMI robust design. The first 5 problems in Fig. 3.10 (a) are related to wiring and solution proposals are given in (b). A very robust, but expensive, solution to EMI propagation through wiring is the use of optical fibers instead of regular wires. Optical fibers, since electrically isolating, cannot receive or conduct CM or DM noise and are therefore an excellent barrier against conducted EMI.

Inter-system EMI control techniques are grouped in four categories: frequency, time, location and direction management. [14]
Frequency management intends to control emission of noise transmitters and improve the response of receivers to such noise. At the transmitter side this would mean to limit the frequency spectrum, i.e. longer pulse rise or fall times. EMI performance can be improved simply by changing the transmitters or receivers frequency such that the transmitted noise is less likely to interfere with the receiver.
Time management refers to applications where information is passed between systems. Examples for time management techniques are minimizing the transferred data or only transfer it in short bursts to reduce the time in which the receiver is susceptible to EMI. Another example would be to interleave the ADC sampling or transfer of data with the switching of a converters main switch such that these sensible operations are done while no switching occurs and thus cannot be disturbed by it.
In Location management, the position of the victim circuit is considered with respect to all potential noise sources in the environment. Location management is very significant as radiated EMI is reduced greatly with distance. Additionally, any obstacles between noise source and receiver further reduce the degree of interference. For example, a busbar which is placed directly on top of a HB module can act as a shield for components in direct line

above it.
Finally, direction management is done by considering the direction and attitude of an electromagnetic signal and arranging the receiver's potential antennae, e.g. loops formed by traces on a PCB or the mounting direction of the PCB itself, in a way that they are less influenced by the interference signal. A concrete example would be to reduce the normal component of the magnetic flux through a loop and thus reduce the induced voltage. Twisted pair wires are also an example of direction management, as the loops formed by the wound wires cancel each other's induced DM currents.

A further summary of methods for reducing EMI emissions, including an evaluation of complexity, cost and time, is given in Fig. 3.11 from [14]. Although they are mentioned as methods for EMI reduction, most of these methods apply to improvement of EMI robustness on the noise receiving side as well.

Method	Complexity	Cost	Time
1. Revise PCB Layout	Medium	Low	High
2. Add Components (Filters)	Medium	Medium	Medium
3. Change Crystal Frequency	High	Low	High
4. Rewrite Software	High	Low	High
5. Add Shielding	Low	High	Low
6. Relocate PCB	Low	Low	Low
7. Change IC Supplier	High	Medium	Medium
8. Fail EMC Qualification—Don't Sell Product	High	High	High

Figure 3.11: Evaluation of EMI reduction methods

Finally, [16] summarizes most, if not all, of the known EMI reduction techniques in electronic systems and can be consulted for any specific problem. Reading on proper circuit design for EMI resilience or reduction is given in [17–22].

An example of an application of the principles discussed in this section is given in [23]. A high dv/dt trace caused heavy noise in the voltage divider it passed underneath. By adding a filter capacitor on the voltage sensing side its bandwidth was limited and noise above the frequency range of interest was reduced. Then, location management was done by increasing the distance between the noisy trace and the voltage divider circuit to reduce coupling. Furthermore, the effective overlapping area between the two traces was reduced (improvement of PCB layout) which led to a further improvement of the situation. Shielding was also applied to get rid of the remaining noise but then removed

due to voltage isolation concerns. Filtering was also applied by the means of chokes in [24] to reduce the CM noise on a voltage sensing line.

3.6 Conclusion

The conclusion of the literature review is that significant conducted and coupled EMI is to be expected in this application of SiC HB modules in an MMC. Since the cell controller has to be operated in close vicinity to heavy noise sources, significant EMI mitigation efforts are expected to be required and therefore justified. Generally, the same EMI mitigation techniques are available for WBG applications as in conventional Si applications, but more effort has to be made in the design of filters and the PCB. Also, inter-system EMI control techniques such as frequency, time, location and direction management have to be carefully applied in order to reduce the influence of coupled and radiated EMI as much as possible. Finally, the abundant use of optical fibers and shields has to be considered in order to prevent noise propagation and protect sensitive devices, which can lead to a significant increase of cost.

4 Circuit design and implementation

4.1 Concept

The block diagram in Fig. 4.1 shows the cell controller and its neighboring components which together form a switching cell. It also presents the concept which was devised for the cell controller with the goal of achieving a very high CM noise immunity, as this form of noise is expected to be very intensive. The controller IC is placed together with all required peripherals, optical transmitters and receivers on a distinct board, the controller board. As the GND connections indicate, it is galvanically isolated from all other components and only communicates through optical fibers. It is supplied from the main or auxiliary power supply (APS) which provides galvanic separation to the gate drivers and cell capacitor. Optical fibers are an absolute barrier against CM noise, but the isolation barriers in the APS and the controller power supply employ a parasitic capacitance which can conduct CM noise, so additional filtering is required.

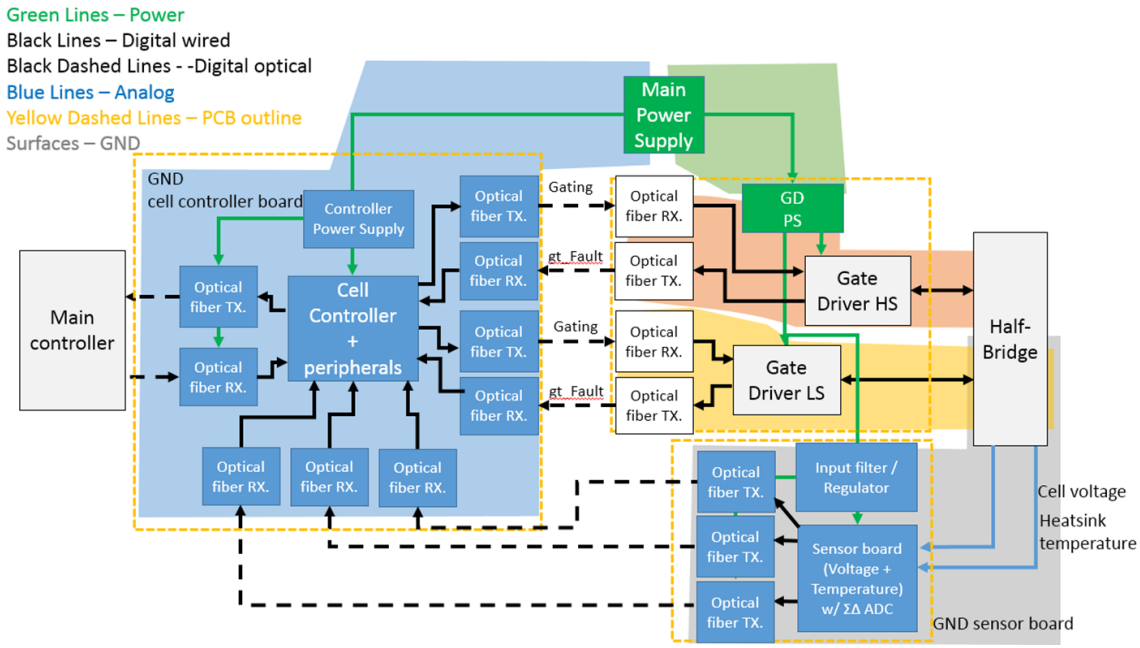


Figure 4.1: Block diagram of the cell controller (blue blocks) and its neighboring components including ground connections

To achieve proper galvanic separation, between controller and sensor, and thus avoid propagation of noise to the controller, it was decided to build a separate board, the sensor board. It measures both the cell capacitor voltage and heat sink temperature. The board is supplied from the low side (LS) gate driver, because it shares the same GND with the half bridge, and therefore the cell capacitor and the sensor board. The sensor board needs to be on the same GND potential as the capacitor, in order to be able to measure its volt-

age. The ADC data is then transmitted to the controller board via optical fibers. Since the sensor board is going to be placed in the vicinity of the half bridge and has a direct connection to it and the gate driver supply, heavy EMI can be expected, which should be mitigated through a number of measures which will be explained in the following sections.

Generally, EMI robustness should be achieved through 4 levels of mitigation efforts, from highest to lowest priority:

1. Use optical isolation wherever possible.
2. Apply appropriate filters wherever optical isolation is not possible.
3. Consider radiation loops from the main power circuit, avoid large receiver loops on the PCB and reduce parasitic capacitances and inductances as much as possible.
4. Shield sensitive circuit components.

4.2 Sensor board circuit design

4.2.1 Target specifications

Based on the specifications and requirements given in chapter 2, the following target specifications were devised for the sensor board:

- Voltage measurement range: 0 - 6.5 kV
- Temperature measurement range: -10 - 160°C
- Sampling rate f_s: 20 kSps
- Measuring bandwidth (-0.1 dB): 5 kHz
- Resolution: >=12 bit
- Maximum power consumption: 1.2 W
- Galvanically separated from the cell controller board

The voltage measurement range was determined by the maximum expected cell capacitor voltage of 6 kV with a small safety margin. The temperature measurement range was determined based on the nominal operating temperatures and the typical measurement ranges of available temperature sensors. Also, the MMC might eventually be used outside as well, where temperatures down to -10 °C might be expected. The sampling rate and bandwidth are a result out of the requirement to be able to measure the switching ripple of the cell voltage while filtering noise and nuisance signals as much as possible. The resolution requirement was set by the responsible for the main controller and the maximum power consumption is limited by the capabilities of the LS gate driver supply.

4.2.2 ADC and optical interface selection

As a first step of designing the sensor board circuit, an ADC (analog to digital converter) and optical interface were selected. Selection criteria were EMI robustness, power requirements and cost, in that order. Six different alternatives were devised and summarized in table 4.1. The EMI robustness was estimated based on information from data sheets and previous experience with certain components and designs. Note that the power and cost given in this table only refer to the specific set of ADC and optical interface, without any additional circuitry.

Table 4.1: Comparison of ADC and optical interface alternatives

Nr.	Description	ADC	Opt. Interface	Comment	EMI robustness	P [mW]	Cost [$]
1	Delta-Sigma ADC Manchester coded + fibers	1x ADS1202	2x AFBR 1624	low input voltage range +-230 mV	medium	405	48.4
2	Delta-Sigma ADC Manchester coded + optocoupler	1x ADS1202	2x RV1S9960A	low input voltage range +-230 mV, optocoupler has isolation capacitance of 0.6 pF	medium	155	21.42
3	Voltage controlled oscillator + optocoupler	2x LM331	2x RV1S9960A	frequency range to 10 kHz, slow readings, sensitive to noise	low	110	16.84
4	Delta-Sigma ADC 2 data 1 CLK + fibers	1x ADS1209	3x AFBR1624	input voltage range +-2.3 V	excellent	540	62.73
5	Microcontroller as ADC + UART via fib ers	1x STM32L021D4	1x AFBR1624	input voltage range +3.3 V, highly flexible	good	118.8	19.18
6	Microcontroller as ADC + UART via optocoupler	1x STM32L021D4	1x RV1S9960A	input voltage range +3.3 V, highly flexible	medium	36.3	5.69

Although power consumption and cost of the design should be controlled, it was concluded that both the power and cost of either of the alternatives lies within specifications and project scope. For this reason and due to its best expected EMI robustness, alternative number 4, the delta-sigma ADC ADS1209 with 2 data and 1 CLK line via optical fibers was selected.

The delta-sigma ADC is a suitable candidate because it transforms the analog mea-

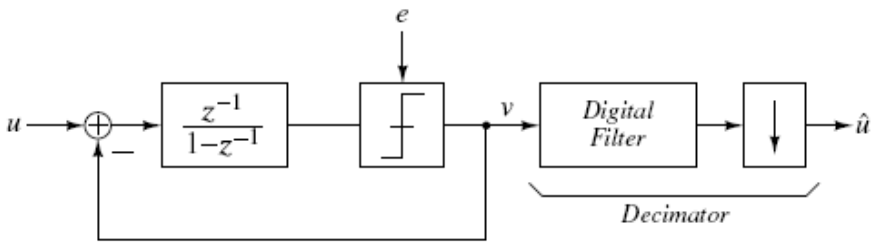


Figure 4.2: System model of an ADC with a first-order delta-sigma modulator [25]

surement signal into an oversampled modulated digital bit stream, which can easily be transported via an optical link without being influenced by noise. The bit stream is then demodulated on the controller side with a digital demodulator. Additionally, the ADS1209 features differential inputs and therefore provides improved CM noise rejection. Fig. 4.2 shows the model of a first-order delta-sigma modulator including the demodulation principle. Another advantage of this modulator type is that its oversampling approach causes noise to be pushed to higher frequencies where they can then be filtered out more easily.

This effect is called noise shaping. More information on delta-sigma ADCs can be found in [25, 26].
For the optical interface, the AFBR 16xx/26xx series optical TX/RX components were selected. They feature baud-rates up to 50 MBd and reduced power consumption compared to other optical TX/RX components on the market.

4.2.3 Circuit principle

Based on the selected ADC and optical interface, a circuit principle for the sensor board was developed. As seen in Fig. 4.3, the voltage and temperature signals are conditioned on the sensor board, modulated with the delta-sigma modulator at a 10 MHz clock and then transferred together with the clock signal (CLK) to the cell controller board. There, the modulated bit streams are demodulated by a digital decimation filter with low pass characteristics. The CLK signal is required for the demodulator to correctly interpret the bit streams. The implementation of the filter is discussed in chapter 6.

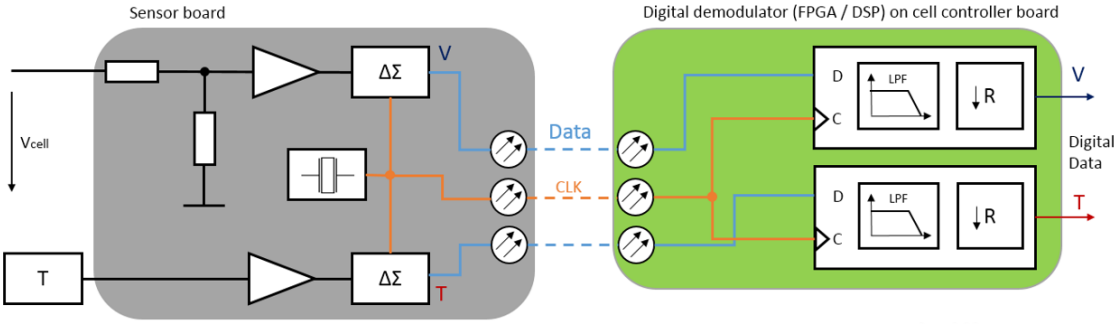


Figure 4.3: Block diagram of the sensor board circuit principle

As mentioned before, this approach is expected to provide a strong resilience against EMI. Furthermore, great flexibility is achieved through the implementation of the digital filter on the controller. Effective sampling rate, resolution and transfer characteristics can be modified as required by the application.
A short online research on isolated voltage measurement showed that a similar approach has been done before by [27], where such a sensor is used for the voltage and current measurement in a medium voltage dc-dc converter. Although no concrete information about the achieved EMI robustness is given, a good ADC performance with a signal to noise and distortion ratio (SINAD) of 68.8 dB and an effective number of bits (ENOB) of 11.1 bit has been achieved at a sampling rate of 156.25 kSps when measuring a noise-free function generator test signal. Based on this information, it can be expected that the sensor built in this project will achieve the previously mentioned specifications.

The following sections explain the single subcircuits of the sensor board. For the full circuit diagram, refer to the Appendix.

4.2.4 Voltage sensor circuit

Fig. 4.4 shows the whole voltage sensor circuit before the ADC. It is comprised of a bandwidth-limited voltage divider and a signal conditioning circuit. The voltage divider has a ratio of 1:1363 and is made up from seven 1 W high voltage resistors which have an operating voltage of 3.5 kV. They provide enough voltage sustain for the maximum input voltage of 6.5 kV and their power loss rating is high enough to avoid significant changes of their resistance values due to self heating. The capacitor C35 creates a low pass behavior of the divider with a cut-off frequency of 72 kHz which leads to a -0.1 dB bandwidth of 5 kHz. For an input voltage of 6.5 kV the dividers output voltage V_{do} is 4.8 V.

The voltage divider output is handled as a differential signal in order to be able to use the

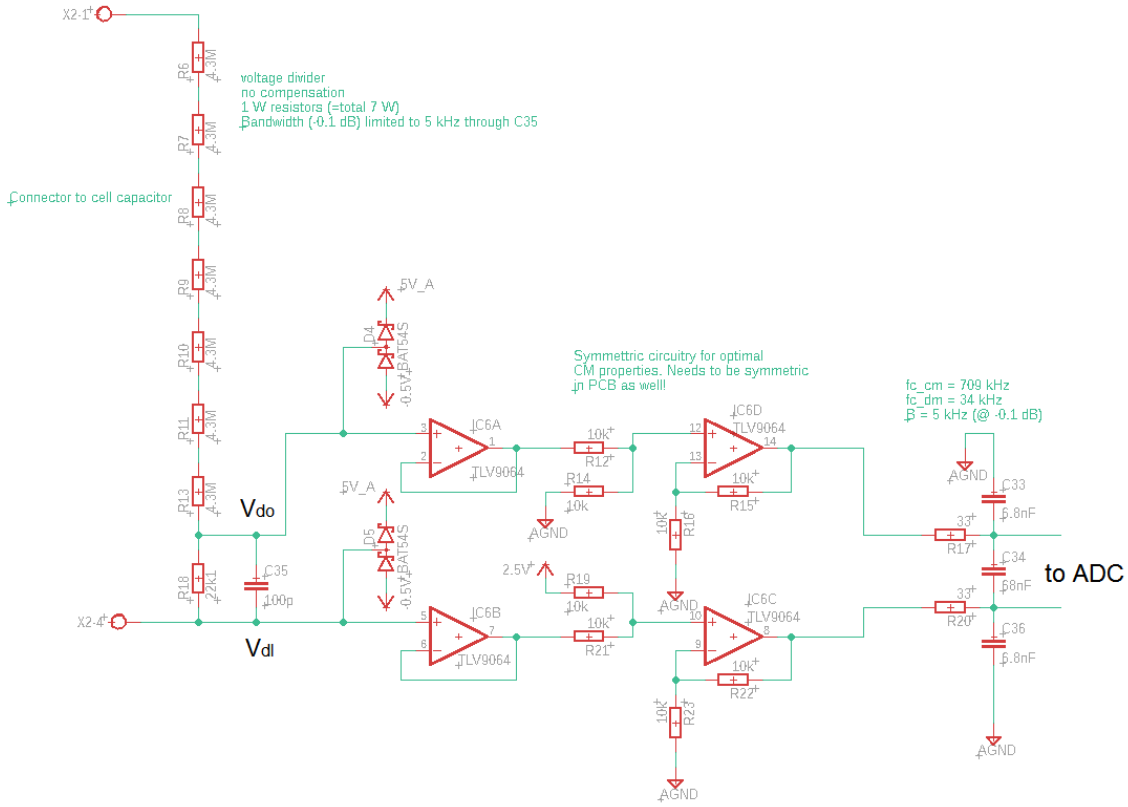


Figure 4.4: Voltage sensor circuit

CM noise rejection of the ADC's differential input and thus achieve improved noise immunity. A small negative supply rail of -0.5 V is provided for this purpose as well. The ADC (ADS1209) has a differential input linear range of $\pm 2.3V$ and a maximum input range of $\pm 2.5V$. Since the measured voltage signal cannot become negative, it has to be extended into the negative range artificially. This is done by adding 2.5 V to the lower signal V_{dl}. As a result, the ADC will see a differential input voltage of $V_d = (V_{do} - (V_{dl} + 2.5V))$. Since V_{do} ranges from 0 to 4.8 V and V_{dl} stays around 0 V, V_d will vary between -2.5 and +2.3 V. While the reduced linearity in the lower input voltage range is negligible, the voltages of main interest are in the ADC's linear region.

IC6C performs this operation through a non-inverting adding circuit which is generally

described by Eq. 4.1

$$V_{out} = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2} \cdot (1 + \frac{R_f}{R_N}) \tag{4.1}$$

where V_1, V_2 are the input voltages, R_1, R_2 are the respective input resistors (i.e. R12/R14 and R19/R21 in the circuit above), R_f is the resistor in the feedback path (i.e. R15, R22 in the circuit above) and R_N refers to R16, R23. In order to maintain symmetry, which is important for CM noise rejection, the same circuit is implemented for the V_{do} signal with IC6D, with the difference that 0 V (AGND) is added. IC6A and IC6B are buffers that avoid loading of the voltage divider which would result in a distortion of the divider ratio. A CM/DM filter with a -0.1 dB bandwidth of 5 kHz is added before the ADC input. It has a common mode cut-off frequency of 709 kHz and a differential mode cut-off frequency of 34 kHz. This filter functions as an analog anti-aliasing filter to avoid frequencies above the modulation rate of 10 MHz.
The diodes D4 and D5 are Schottky-diodes which protect the OPAMPs (TLV9064) by limiting the voltages at their inputs to the supply rails $\pm 0.3V$ which is within their specification.

4.2.5 Temperature sensor circuit

The temperature is measured with a series linearized negative temperature coefficient thermistor (NTC), which was inspired by [28]. The circuit is shown in Fig 4.5, and the NTC is connected at X3. Immediately at the NTC connector are two transient voltage suppression (TVS) diodes (D7, D8) which protect the circuit in case of any high voltage breakdown to the NTC which is connected to the heat sink of the half-bridge module. C39 and C40 are buffer capacitors which should reduce noise coupled into the supply rails through the NTC wires. R28 is the series linearization resistor, which is followed by a passive low pass filter with a cut-off frequency of 1.5 Hz. This filter removes most noise from the signal path and can have this low cut-off frequency since the temperature signal is very slow. D6 offers additional protection to the OPAMP input against a potential overvoltage. The OPAMP circuit around IC6 shifts the sensor signal into the required voltage range of around 0.2 to 4.8 V for temperatures from -10 to 160°C. Again the differential input voltage for the ADC needs to be shifted down by 2.5 V to use its full input range. Since the temperature signal is single ended, this is simply done by wiring 2.5 V to the ADC's negative input. The 2.2 $k\Omega$ resistors R26 and R29 are added to increase the current flow on this signal line and thus improve immunity against coupled noise.

The resistance of the NTC is a function of the temperature T and given by

$$R_{NTC}(T) = R_{25} e^{B(\frac{1}{T+273.15} - \frac{1}{25+273.15})} \tag{4.2}$$

where R_{25} is the NTC's resistance at 25 °C and B is a material constant. The output of

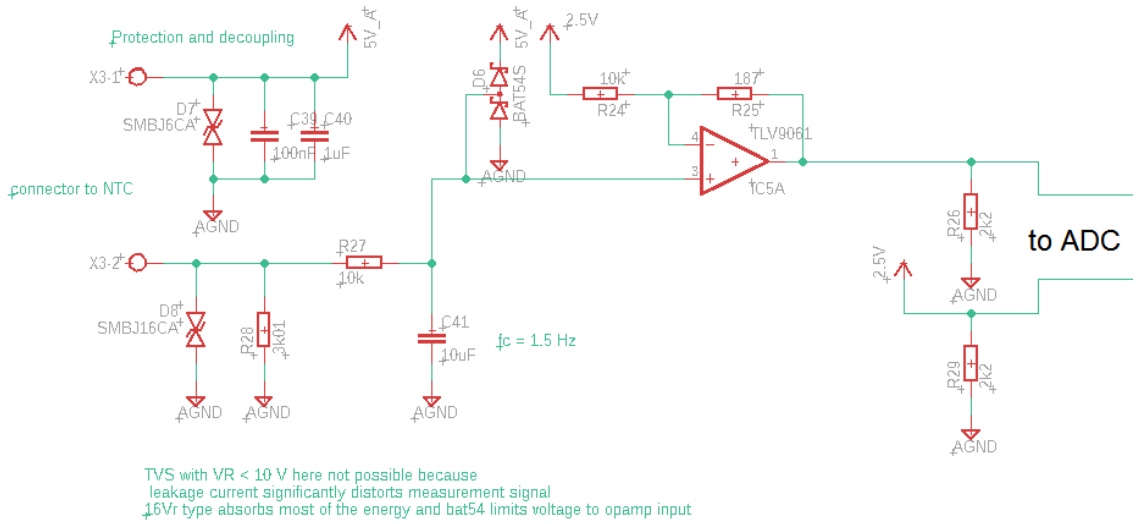


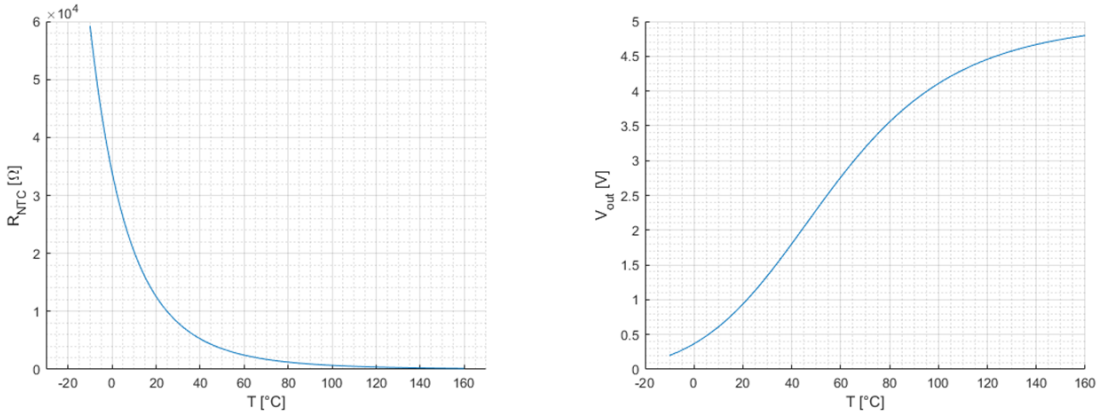
Figure 4.5: Temperature sensor circuit

the linearization circuit is given by

$$V_{out}(T) = 5V \frac{R_{28}}{R_{28} + R_{NTC}(T)} \frac{R_{24} + R_{25}}{R_{24}} - 2.5V \frac{R_{25}}{R_{24}} \tag{4.3}$$

The NTC resistance curve and the circuit's output voltage are given in Fig. 4.6. It can be seen that the NTC resistance is highly nonlinear vs. the temperature, which justifies the need for linearization in order to get a good resolution over the whole measurement range. The linearized output voltage is only really linear in the range from 20 to 80°C, but even the nonlinear regions at the edges are much better suited than the NTC's resistance curve. A sensitivity of 30 to 45.5 mV/K is achieved between 20 to 90 °C which is within the main operating temperature range.

The voltage signal is then modulated by the delta-sigma modulator and transferred



(a) NTC resistance curve (b) Linearization circuit output voltage

Figure 4.6: NTC resistance and linearization circuit output voltage versus temperatures

to the controller, where it is filtered and decimated. A lookup table (LUT) has the curve in Fig. 4.6(b) stored and is then used to link the demodulated voltage value to the temperature. The implementation of the LUT is discussed in section 6.3.

The used NTC is a TDK B57703M0103A017 type with an R_{25} of 10 $k\Omega$ and a B value of 3988 K.

4.2.6 ADC circuit

Fig. 4.7 shows the circuitry around the ADC ADS1209. The circuit follows the data sheet recommendations. All supply pins are decoupled with 100 nF and 1 uF ceramic capacitors. The reference voltage pins REFINA and REFINB are buffered with 100 nF. Test points were added to the input signal lines for testing purposes. CLKSEL is tied to GND which signals the IC to use the external clock input CLKIN.

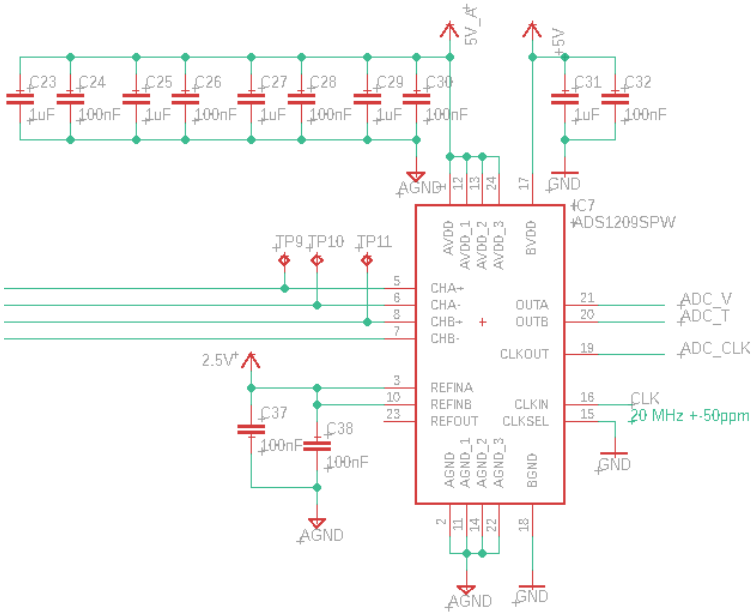


Figure 4.7: ADC circuit

4.2.7 Optical TX, indicator and clock circuits

The circuits for the optical transmitters, status indicators and the clock are shown in Fig. 4.8. The optical transmitters AFBR-1624 are supplied through a LC pi filter as proposed by their data sheet. The filter uses the same components as the analog to digital rail filter, thus has a resonant frequency of 15 kHz as well, which is well below the transmitter operating frequency. A 4.7 $k\Omega$ pull-down resistor is added to the DIN pin as specified by the data sheet. It improves the signal's integrity and resilience against noise.

The circuit around IC4 is used for status indication. It is a monostable multivibrator which re-triggers on every positive flank in the modulated data bit streams from the delta-sigma modulator (ADC_V and ADC_T). As long as its input is re-triggered within the time

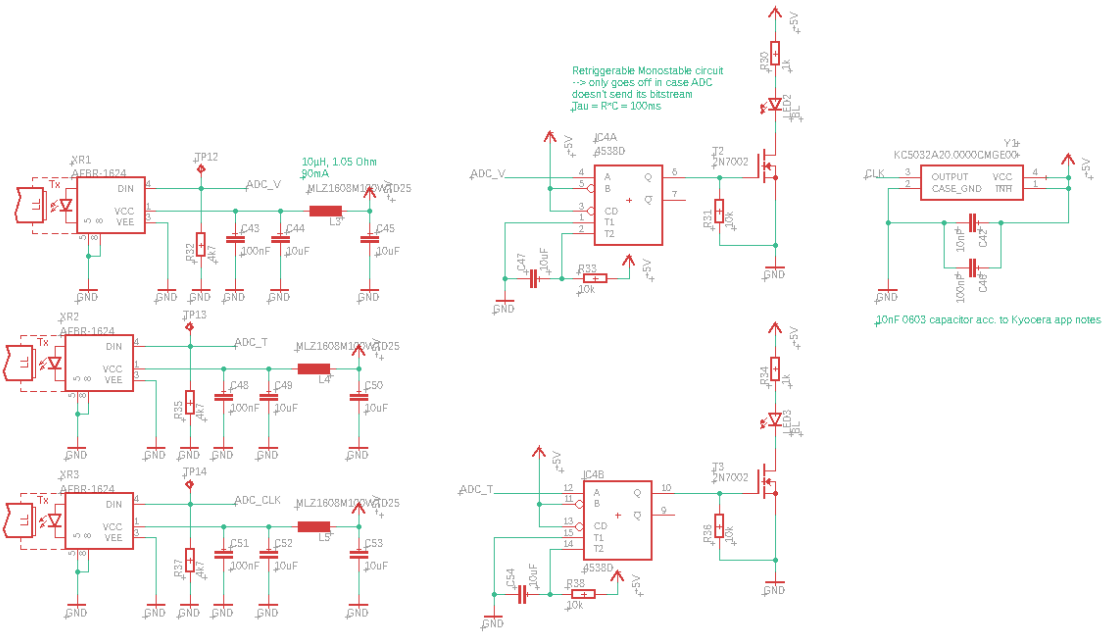


Figure 4.8: Optical TX, indicator and clock circuits

constant of 100 ms, the output stays high, such that the transistor (T2/T3) and thus the LED (LED2/LED3) is on. This way, a failure of the ADC or the signal conditioning circuits is indicated directly on the PCB. Finally, the clock is provided by a KC5032A20 clock source IC. It operates at 20 MHz ±50 ppm and requires a current of around 7 mA. The supply rail is decoupled through a 10 nF, as specified by the manufacturer's application note. An additional 100 nF ceramic capacitor was added for improved voltage stability. The 20 MHz clock is internally decimated down to 10 MHz in the ADC.

4.2.8 Supply circuit

A power estimation of the sensor board circuit was performed before designing the supply circuit. Table 4.2 summarizes the estimation of the circuit's main components. P is the power lost on a single component of a certain type and P_{tot} the total loss for all components of that type. It can be seen that a total power of 587.5 mW, or a total current of 117.5 mA at 5 V is expected to be required for the circuit's operation.

In further considerations, a small safety margin is added to account for any remaining circuit components which results in 125 mA or 625 mW.
In order to achieve good efficiency and a noise free supply voltage, it was decided to use a DC/DC converter to efficiently bring the input voltage of 15 V down to 5.15 V and then add a low dropout linear regulator (LDO) to get a noise free 5 V supply rail. The power loss across the LDO is given by $(5.15-5)\ V \cdot\ 125mA = 18.75mW$. The used DC/DC converter (Würth Magic Power Module 17791063215) has an efficiency of 75 % which leads to a total estimated power requirement of $(625 + 18.75)\ mW/0.75 = 858.3\ mW$. This value is well below the allowed maximum of 1.2 W. Furthermore, the power requirements given in the

Table 4.2: Power estimation of the sensor board circuit components

Component	#	I [mA]	V [V]	P [mW]	P_{tot} [mW]
Opt TX AFBR 1624	3	31	5	155	465
ΔΣ ADC ADS1209	1	15	5	75	75
TLV906x quiescent current per channel	4	0.5	5	2.5	12.5
KC5032A20 clock IC	1	7	5	35	35
SUM		117.5			587.5

table above are maximum values as specified by the components' data sheets. The actual power consumption under nominal operation should be in the range of 600 to 700 mW. For example the nominal operating current for the optical TX AFBR 1624 is stated as 21 mA. The complete sensor board supply circuit is given in Fig. 4.9. 15 V are provided to

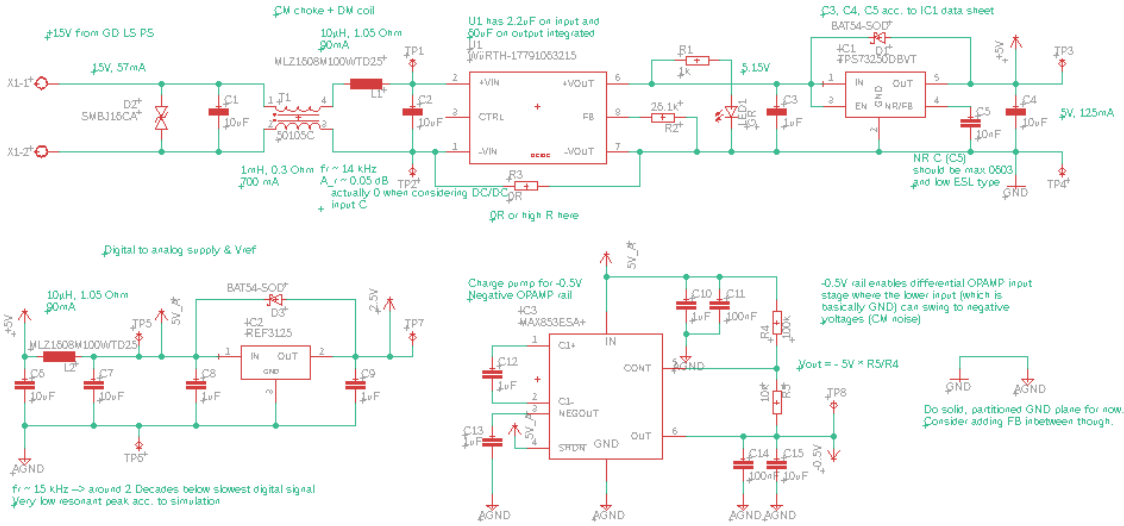


Figure 4.9: Sensor board supply circuit

the board from the lower side gate driver power supply. The TVS diode D2 protects the input against transient overvoltages. It is followed by an input filter which is formed by a CM choke and a DM coil. The filter's resonance frequency is at around 14 kHz and it has a damped frequency response. This filter is intended to suppress any high frequency CM or DM noise which might propagate to the sensor board through the wire connection to the gate driver board. The GND pins of the isolated DC/DC converter are connected since the board needs to be at the same GND potential as the cell capacitor, for reference see Fig. 4.1. Even though the GNDs are connected, the isolation of the DC/DC converter still works on the +VIN/VOUT pins which further hinders propagation of noise and provides safety to the rest of the circuit in case of a failure on the primary side. The digital part of the circuit is directly supplied from the 5 V of the LDO (TPS73250). A LC pi filter separates the analog from the digital supply rail. It features a resonant frequency of 15 kHz

with a very small resonant peak. This resonant frequency is more than 2 decades below the lowest appearing digital signal on the sensor board, which is the 10 MHz clock signal of the ADC, and should therefore provide a clean supply for the board's analog circuitry.

A 2.5 V rail is created with a REF3125 reference voltage IC. It is used as an accurate reference voltage for the ADC and the signal conditioning circuitry. Finally, a -0.5 V rail is provided through a MAX853 charge pump. As mentioned before in 4.2.4, this small negative rail allows the cell capacitor's negative terminal voltage to go slightly negative, e.g. due to CM noise, which should improve the differential ADC's overall common mode rejection. For the first prototype design, the analog and digital grounds were connected in a solid GND plane, which will be explained in more detail in chapter 5.2. Additionally, all IC supply pins are decoupled with at least a 100 nF ceramic capacitor, with a 1 uF ceramic capacitor added to every analog IC.

4.3 Cell controller board circuit design

4.3.1 Target specifications

Based on the specifications and requirements in chapter 2 and the sensor board circuit design, the following target specifications were devised for the cell controller board circuit:

- Gate driver signals: 2 opt. TX for PWM output and 2 opt. RX for fault input
- Main controller (MC) communication: 1 opt. TX for data transmission and fault signaling to MC, 1 opt. RX for switching data and fault signaling from MC, around 10 MBd data rate each
- Sensor board signals: 3 opt. RX for 2 data and 1 CLK signal
- Configuration interface on board for easy reconfiguration
- Parallel handling of all tasks
- Maximum power consumption: 6 W
- Galvanically separated from every other component of the switching cell

4.3.2 Controller IC selection

The first step in designing the cell controller board circuit was to select a controller IC. In the initial stages of the project, the information gather in table 4.3 was used to determine which type of controller IC will be the most suitable for the tasks specified in chapter 2 and section 4.3.1. Since the controller IC is required to handle its tasks in parallel at high clock rates, both the DSP and microcontroller are not suited. They only operate sequentially and only a quasi-parallelization is possible through the use of interrupts, which is not satisfactory for this application. The CPLD, although cheap, flexible and

robust, is disqualified because no on-die hard IPs (intellectual property cores), such as a PLL (phase locked loop) which is required for internal clock generation, are available and the amount of available logic resources is usually quite small.
The FPGA was chosen because it provides a far higher number of logical resources and a variety of on-die IPs. Additionally tools are available for FPGA in the loop simulation which allows fast testing of FPGA firmware designs in conjunction with a simulation, which is especially useful for working in home office. The only downside of FPGAs is that most ICs need to load the configuration from an external ROM, which takes several ms of time and can lead to issues if the FPGA shuts down unexpectedly during operation. However, newer generation FPGAs are available which have the ROM on-chip and are able to boot up almost as fast as CPLDs.

Table 4.3: Comparison of different controller ICs' properties

CPLD	**FPGA**
Instant on as configuration is 'hardwired'	Loads configuration from external ROM (several ms), but on-chip ROM available
Usually cheaper	More pricy
Small amount of logic resources (some 500 flip flops)	Much more resources (millions of flip flops)
No on-die hard IPs available	Variety of on-die dedicated hardware (PLL, DSP blocks etc.)
	FPGA in the loop available f. home office developing
DSP	
Optimized for signal processing	**Microcontroller**
Faster integer and floating point operations	Usually quite robust
Input/output device	Multifeature device
Less robust	Usually slower than DSPs

Based on this decision, the DE0-Nano development board with a Cyclone IV EP4CE22F17C6N FPGA was selected for developing the basic functionality of the cell controller firmware. After the implementation of the basic functions, it was determined that the FPGA for the cell controller needs to fulfill at least the following requirements:

- Minimum number of logic elements (LEs): 5493
- Minimum number of memory bits (RAM): 6228
- Minimum number of registers: 3897
- Minimum number of 9 bit multipliers: 52
- Minimum number of PLLs: 1

The implementation of the firmware is explained in detail in chapter 6.
Based on the specifications above, the intel MAX10 FPGA 10M16SAE144I7G was selected. It features 16000 LEs, 459 kbits RAM, 2369 kbits user flash memory, 45 18x18 multipliers and 1 PLL. This FPGA is believed to provide sufficient headroom for the full firmware and any additional functions which might be added in the future.

The following sections will explain the single subcircuits of the cell controller board. The complete circuit schematic can be found in the Appendix.

4.3.3 Cell controller signals and FPGA Pinout

Table 4.4 is a summary of the signals going into and out of the FPGA, and thus are present on the cell controller board. It includes the pin locations, I/O Bank, VREF Group and I/O Standard as defined in the intel Quartus software. The I/O Bank indicates the general location of the pin on the chip. The VREF group indicates which pins work at the same reference voltage, should a voltage referenced I/O standard be used. As it can be seen, all pins operate on the 3.3-V LVTTL standard, which is not a voltage referenced I/O standard per definition. The ST_LED_xx status signals are used to switch on the status LEDs on the board and were named to match the respective LED identifiers. It was done this way for generality and to make it easier to link a certain status to a certain LED, should it be required to make changes in the indicated statuses. The pinout was determined such

Table 4.4: Cell controller signals and FPGA pinout

Signal	Direction	Location	I/O Bank	VREF Group	I/O Standard	Description
JTAGEN	Input	PIN_15	1B	B1_N0	3.3-V LVTTL	JTAG Configuration
TMS	Input	PIN_16	1B	B1_N0	3.3-V LVTTL	JTAG Configuration
TCK	Input	PIN_18	1B	B1_N0	3.3-V LVTTL	JTAG Configuration
TDI	Input	PIN_19	1B	B1_N0	3.3-V LVTTL	JTAG Configuration
TDO	Output	PIN_20	1B	B1_N0	3.3-V LVTTL	JTAG Configuration
ST_LED_2	Output	PIN_27	2	B2_N0	3.3-V LVTTL	Status indication GR
ST_LED_3	Output	PIN_28	2	B2_N0	3.3-V LVTTL	Status indication RE
ST_LED_4	Output	PIN_29	2	B2_N0	3.3-V LVTTL	Status indication YE
ST_LED_5	Output	PIN_30	2	B2_N0	3.3-V LVTTL	Status indication YE
ST_LED_6	Output	PIN_32	2	B2_N0	3.3-V LVTTL	Status indication BL
ST_LED_7	Output	PIN_33	2	B2_N0	3.3-V LVTTL	Status indication BL
ST_LED_8	Output	PIN_38	3	B3_N0	3.3-V LVTTL	Status indication BL
ST_LED_9	Output	PIN_39	3	B3_N0	3.3-V LVTTL	Status indication BL
ST_LED_10	Output	PIN_41	3	B3_N0	3.3-V LVTTL	Status indication BL
ST_LED_11	Output	PIN_43	3	B3_N0	3.3-V LVTTL	Status indication BL
MC_RX	Input	PIN_44	3	B3_N0	3.3-V LVTTL	Main controller communication
MC_TX	Output	PIN_47	3	B3_N0	3.3-V LVTTL	Main controller communication
CLK_50	Input	PIN_58	3	B3_N0	3.3-V LVTTL	FPGA main clock
GD_LS_FT	Input	PIN_74	5	B5_N0	3.3-V LVTTL	Gate driver fault signal
GD_LS_GT	Output	PIN_76	5	B5_N0	3.3-V LVTTL	Gate driver gate signal
GD_HS_FT	Input	PIN_79	5	B5_N0	3.3-V LVTTL	Gate driver fault signal
GD_HS_GT	Output	PIN_81	5	B5_N0	3.3-V LVTTL	Gate driver gate signal
SB_ADC_V	Input	PIN_84	5	B5_N0	3.3-V LVTTL	Sensor board data
SB_ADC_T	Input	PIN_86	5	B5_N0	3.3-V LVTTL	Sensor board data
SB_ADC_CLK	Input	PIN_90	6	B6_N0	3.3-V LVTTL	Sensor board clock

that signals are thematically grouped in the different I/O banks which allows for a clear

separation of subcircuits and easier routing in the PCB design. Looking at the FPGA IC from the top, bank 1 is on the left, banks 3 and 4 are on the bottom and banks 5 and 6 are on the right. Some additional configuration pins which do not have to be defined in the FPGA pinout are also on bank 8, which is at the top edge of the IC.

4.3.4 FPGA I/O banks and clock

Fig. 4.10 shows the connections at the I/O banks of the FPGA. Some pins were connected to GND as indicated by the FPGA pin connection guidelines or in order to reduce cross talk between fast signal lines. Most unused pins remain unconnected as stated by the pin connection guidelines.

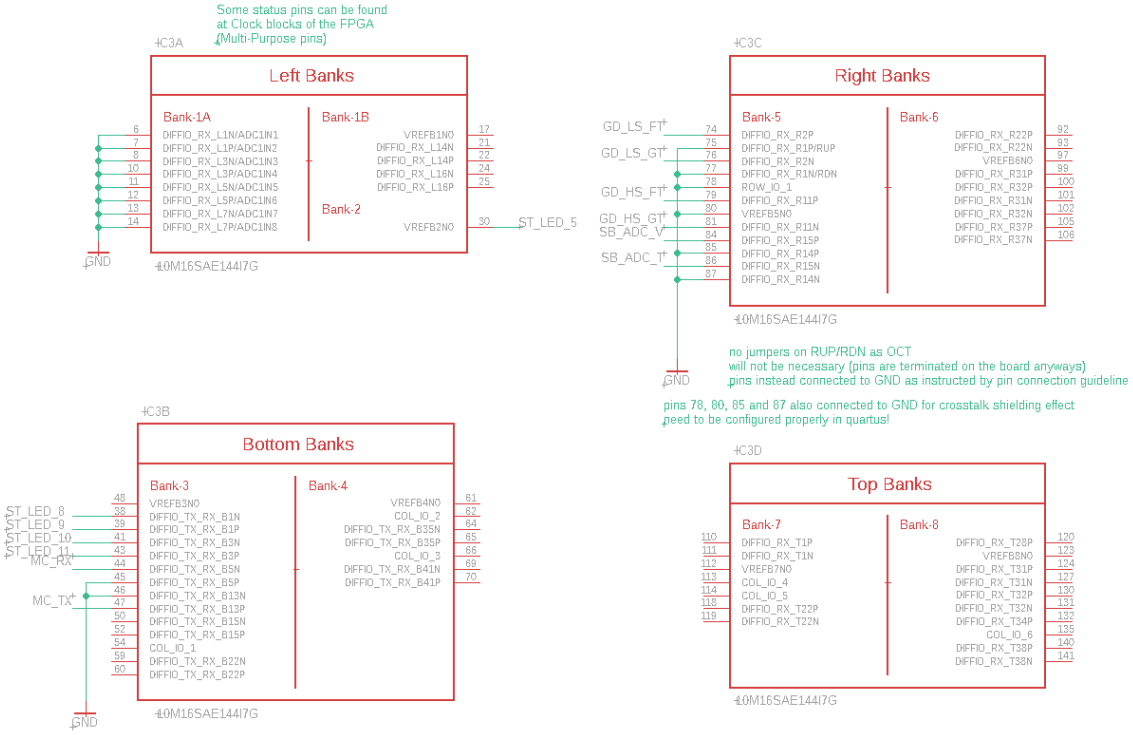


Figure 4.10: I/O Banks of the FPGA

Fig. 4.11 shows the clock bank of the FPGA. Some of the clock pins are used for the status signals instead, while the unused clock pins are connected to GND as indicated by the pin connection guidelines. A clock IC of the same type as on the sensor board is used for the main clock, but with a clock frequency of 50 MHz ± 50 *ppm*. Again, the clock IC is decoupled with a 10 nF and a 100 nF ceramic capacitor. The SB_ADC_CLK signal is routed to the CLK3N input, since it has to be used as clock for the digital decimation filter.

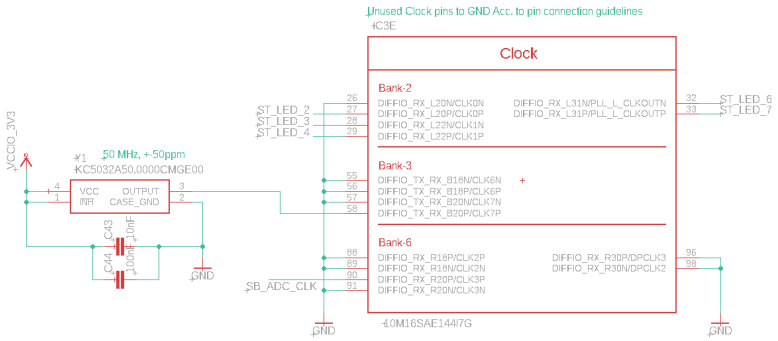


Figure 4.11: FPGA Clock circuit

4.3.5 Indicator circuit

The statuses are indicated simply through LEDs which are driven directly by the FPGA pins. The LEDs require a current of only 2 mA which can be delivered by the FPGA. The circuit is shown in Fig. 4.12. The comment below the circuit explains which status should be indicated by which LED. Jumpers are provided for the IC_OP (IC operates) and the Fault status to allow for an easy connection to a front panel, should one be built in the future.

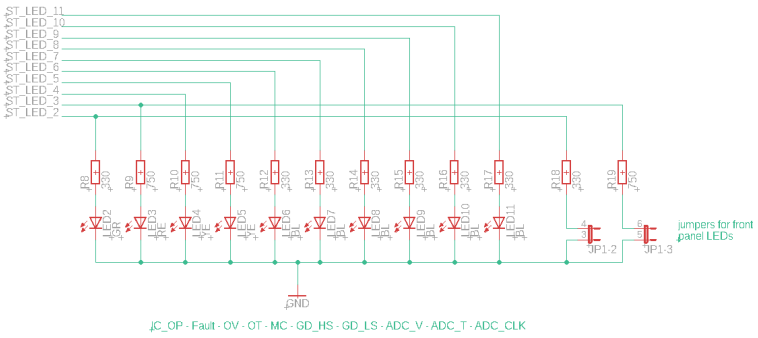


Figure 4.12: Status LEDs at the cell controller board

4.3.6 Optical TX/RX circuit

As it can be seen in Fig 4.13, a total of 3 optical transmitters and 6 optical receivers are installed on the cell controller board. The same types as for the sensor board are used and again the supply filters were designed according to the data sheet recommendation. Additionally, pull-down resistors are added for each receiver. The resistors are placed directly at the FPGA pin in the PCB design.

4.3.7 Configuration circuit

The FPGA can be configured in circuit through the available JTAG interface. A JTAG programmer can be connected to the cell controller board via a 10-pin header. The circuit

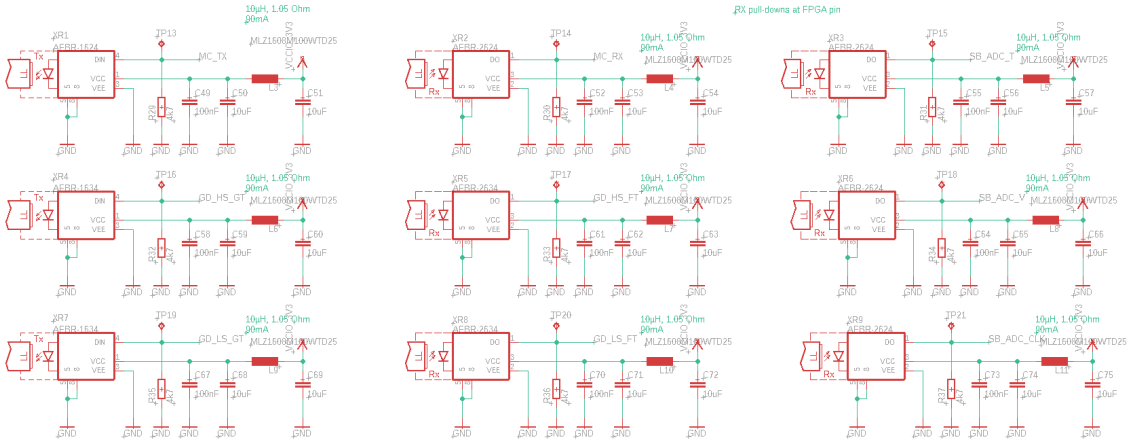


Figure 4.13: Optical TX/RX circuit at the cell controller board

in Fig. 4.14 shows that all JTAG pins (TMS, TCK, TDI, TDO) are protected with capacitors and Schottky-diodes to avoid damaging of the pins through any overvoltages which might occur during the communication with an external programmer through the 'JTAG-IN' connector. All configuration pins on the FPGA were connected as recommended by the pin connection guidelines. A switch is connected at NCONFIG which enables a manual reset of the FPGA, e.g. during debugging. A jumper at CONFIG_SEL allows for the selection of one of two possible boot images.

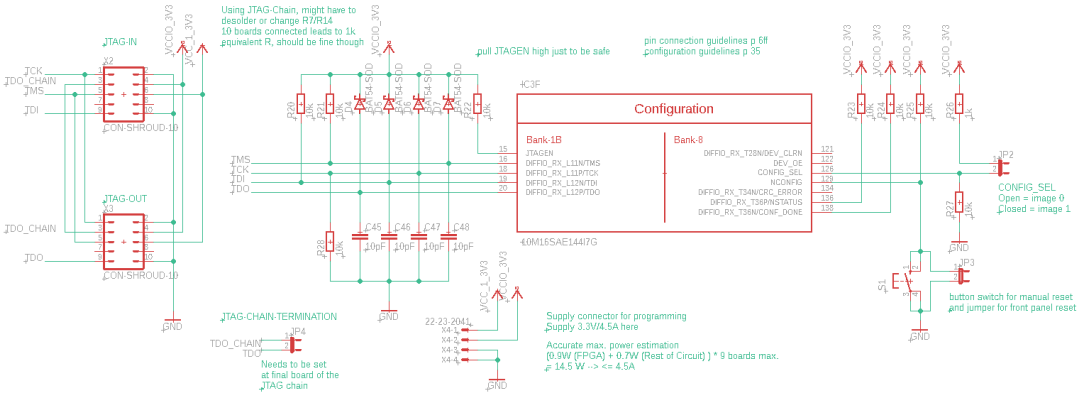


Figure 4.14: Configuration circuit for the FPGA

To allow for batch firmware updating of multiple cell controllers at once, a second connector 'JTAG-OUT' was added to allow the creation of a JTAG chain between multiple cell controller boards. When connecting a programmer to 'JTAG-IN', it sends the configuration data via TDI to the first FPGA. This data is then output on its TDO pin. The TDO signal is then routed to the next FPGA's TDI pin via the 'JTAG-OUT' connector and so on until the last FPGA in the chain has received the configuration data. On this last controller board, the 'JTAG-CHAIN-TERMINATION' jumper needs to be set in order to terminate the chain and feed the last TDO signal back to the programmer which checks whether the original configuration data was passed correctly to every FPGA.

The controller boards cannot be programmed during regular operation, as this would mean to have a non-isolated connection from the MMC cabinet to the outside that can lead to damage of equipment and injury of persons. Therefore, an auxiliary supply is required to supply the cell controller boards for programming. An auxiliary supply, like a switching converter or a battery, can be connected to the header X4 on the first board of the JTAG chain for this purpose. The other boards are then supplied via the supply pins on the JTAG connectors. An estimation of the controller board's power requirement, see section 4.3.8, indicates that around 1.6 W are required from this auxiliary supply for the FPGA and components of a single board. At a maximum of 9 boards connected in a chain, this poses a requirement of 14.4 W or around 4.5 A at 3.3 V for the auxiliary supply. However, at the point of writing this report, the JTAG chain has not been tested yet and it should be possible to further reduce this power requirement by shutting down most FPGA functions and the components on the board during and after programming. To figure this out is a task for the continuing work on this project.

4.3.8 Supply circuit

As for the sensor board, a power estimation was performed before designing the controller board's supply circuit. Table 4.5 summarizes the circuit's main components. It should be noted that the maximum current values for the optical TX/RX were gathered here, while the stated nominal operating currents are in the range of 20 mA. This was done to make sure that the power supply design considers every possibility. The FPGA power dissipation was estimated based on the power analyzer tool provided by the intel Quartus software. The preliminary firmware was compiled and run through this tool. Then a small margin was added to provide some headroom for further functions which might be implemented in the future.

Table 4.5: Power estimation of the cell controller board components

Component	#	I [mA]	V [V]	P [mW]	Ptot [mW]
Opt TX AFBR 1624	3	31	3.3	102.3	306.9
Opt RX AFBR 2624	6	30	3.3	99.0	594.0
Status indication LEDs	11	2	3.3	6.6	72.6
FPGA 10M16SAE144I7G	1	272.72	3.3	900.0	900.0
SUM		567.7			1873.5

It can be seen that the total expected power requirement for the cell controller board is around 1.8 W or 567.7 mA at 3.3 V. When using the optical TX/RXs' nominal operating current, a power consumption of around 1.6 W is expected, as was previously stated in section 4.3.7.

The supply circuit for the cell controller board is given in Fig. 4.15. 18 to 36 V and max.

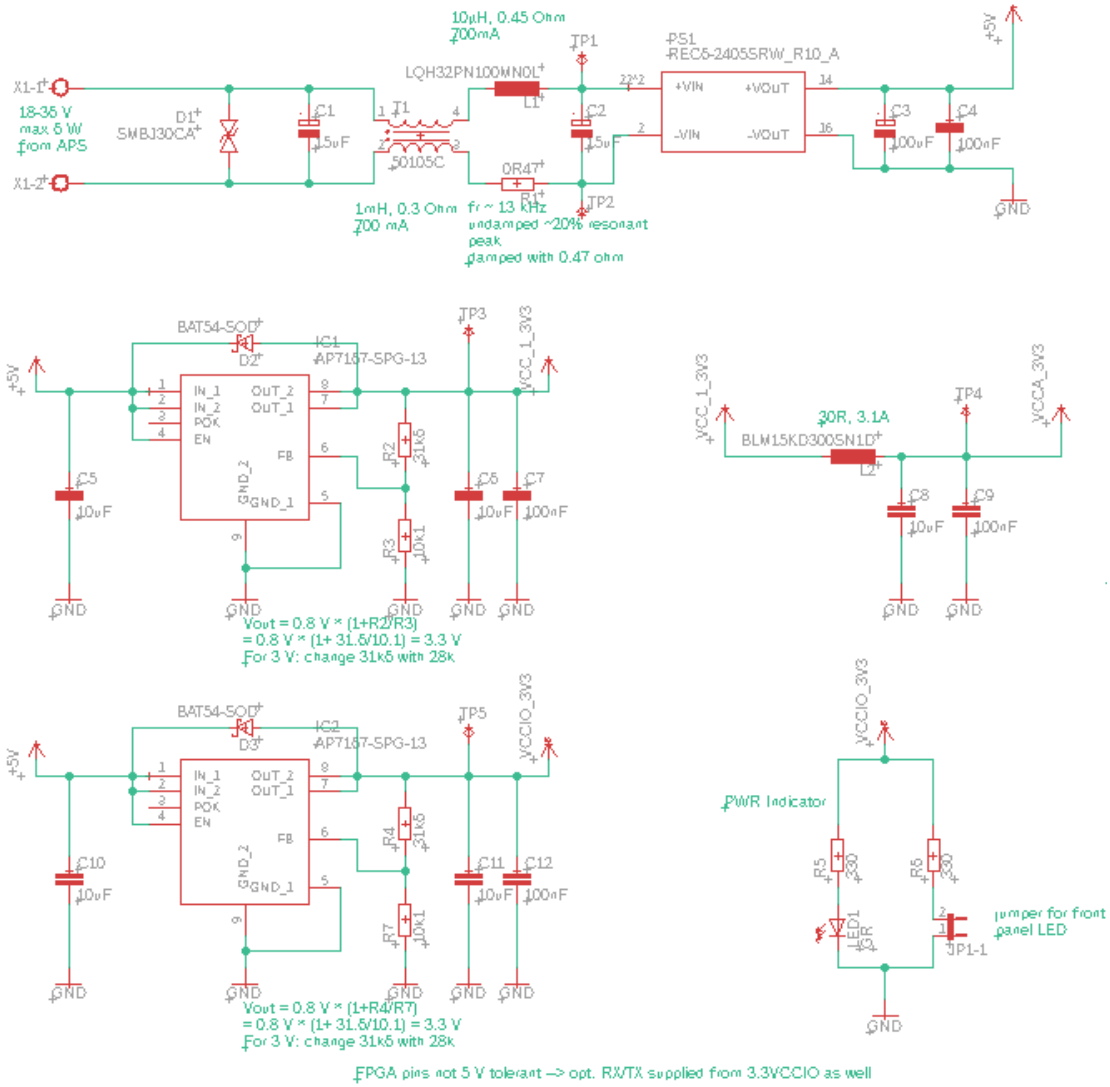


Figure 4.15: Supply circuit for the cell controller board

6 W are provided from the APS. A TVS diode protects the circuit from overvoltages. It is followed by a CM/DM filter, similarly as for the sensor board. It's resonant frequency is in the range of 13 kHz and a damping resistor of 0.47 Ω was added to add additional damping to the filter response. A DC/DC converter with an isolation voltage of 10 kV follows, which provides galvanic separation and brings the input voltage down to 5 V with an efficiency of 80 %. The galvanic separation and small isolation capacitance of around 20 pF also provides a good barrier for CM noise. Two linear regulators are used to provide 3.3 V to the VCC_1 and VCCIO rails of the FPGA. This separation of supplies is required by the FPGA pin connection guidelines. VCC_1 supplies the FPGA's core and logic elements while VCCIO supplies the I/O buffers of its pins. Based on the power estimation above, the total power loss across the linear regulators is $(5-3.3)\ V \cdot 567.7\ mA = 965.1\ mW$. The total required input power therefore is estimated to be $(1873.5+965.1)\ mW/0.8 = 3.55\ W$.

A margin of 2.45 W is therefore available from the APS for the implementation of further functions on the FPGA.

Additionally to the splitting of the VCC_1 and the VCCIO rails, VCCA has to be supplied from VCC_1 through an LC filter. VCCA supplies the internal analog components, which are not used in this design, and the PLL. Finally, an LED is added for a 'power good' status indication.

5 PCB design

5.1 Design considerations

The prototype PCB was designed mostly with 0805 format SMD components since they require less space than through hole components but can still be soldered by hand if modifications are required. Only certain decoupling capacitors or filter components were chosen in the 0603 or 0402 format in order to reduce parasitic inductance and thus improve their HF filtering properties. Wire thickness and via diameter were determined based on the expected current flow on a trace, but generally as thin as possible without risking mechanical issues. Any lines where a low parasitic inductance and/or good coupling to the GND plane are required were designed with generous trace width or as a plane. This includes for example the supply lines to the optical transmitters/receivers, since they are expected to draw high current spikes.
The PCB design was strongly influenced by the EMI literature review in chapter 3. Routing, grounding and component placement are based on personal experience in PCB design and the information provided in [16–20, 22].

5.1.1 PCB layer stackup

PCB layer stackups are listed and evaluated in [19]. The possible stackup models for four-layer and six-layer designs are given in tables 5.1 and 5.2. It can be seen that generally, a six-layer stackup provides the best properties considering decoupling, EMC and signal integrity. However, since the cell controller and sensor board do not have a very high number of signals that needs to be routed, a six-layer stackup was considered to be exaggerated and too expensive for this design. Therefore, a combination of the four-layer model 2 and six-layer model 5 was devised for both boards. The stackup is

1. SIG
2. GND
3. VCC
4. GND/SIG

which is expected to provide good decoupling, signal integrity and EMI robustness. The 4th layer consists mostly of a solid GND plane with only few high speed or less vulnerable signal traces while all vulnerable or analog signals will be routed on the first layer. Since it is currently planned to mount the controller and sensor board above the SiC HB module and the busbar, 3 solid layers, 2 GND and 1 VCC, are provided between the noise source and the vulnerable circuitry which should significantly reduce coupling into signal traces.

Table 5.1: Possible PCB layer stackups on a four-layer PCB [19]

	Model 1	Model 2	Model 3	Model 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal integrity	Bad	Bad	Good	Bad
Self disturbance	Satisfaction	Satisfaction	Satisfaction	High

Table 5.2: Possible PCB layer stackups on a six-layer PCB [19]

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
Layer 1	SIG	SIG	GND	SIG	SIG	SIG
Layer 2	SIG	GND	VCC	GND	GND	GND
Layer 3	VCC	VCC	SIG	VCC	VCC	VCC
Layer 4	GND	VCC	SIG	SIGH	GND	GND
Layer 5	SIG	GND	VCC	GND	Not used	SIG
Layer 6	SIG	SIG	GND	SIG	SIG	SIG
Decoupling	Good	Good	Good	Good	Good	Good
EMC	Bad	Good	Satisfaction	Satisfaction	Good	Good
Signal integrity	Bad	Good	Bad	Good	Good	Bad

5.1.2 Grounding

Grounding is a very important issue in PCB design. A thorough discussion is given in [17] and [18]. A solid ground plane is always recommended and often it is suggested to split it into an analog and digital plane which should be connected only at a single point. This helps reduce the influence of high return currents from digital circuits onto the analog circuits. However, split ground planes also tend to act as slot antennas and radiate EMI, which is not of concern in this design. A greater issue is, that improperly connected split planes or also signal routed across the planes can cause significant noise problems on the PCB and a split plane also has a reduced shielding effect against noise. If it is possible to locally separate the digital from the analog circuitry and no signals have to be routed from the analog to digital part and vice versa, a single solid GND plane might actually be the better option.
The cell controller board is a purely digital circuit, so a solid GND plane was used. The

sensor board incorporates digital and analog circuitry. Due to the considerations above, it was decided to use a solid GND plane and split the board into digital and analog sections as is shown in section 5.2.
A solid GND plane also provides direct current return paths and significantly reduced loop areas, which reduces (electro-)magnetic coupling of DM noise into the circuit.

5.1.3 EMI mitigation efforts in PCB design

A summary of design considerations for EMI mitigation which were followed in the layout design of the controller and sensor board PCBs are:

- Four-layer stackup as discussed in 5.1.1, with analog and vulnerable signals and components strictly on first layer
- Grounding and local separation of layout into analog and digital sections as discussed in 5.1.2
- Proper spacing of high speed signal traces and via stitching to reduce cross talk and coupling from external sources
- Proper placement of supply input filter components to reduce parasitics
- Proper spacing of supply input filter to rest of circuit to avoid coupling effects
- Proper placement of decoupling capacitors according to [19]
- Provide space, mounting pads for shielding if determined to be necessary
- Ensuring equal length and symmetry of differential signal traces and circuitry

5.2 Sensor board

The layout of the sensor PCB is given in Fig.5.1. It can be seen how the board is logically separated from left to right into: supply input filter, digital circuitry, analog circuitry and voltage divider. The GND planes are indicated by the dashed polygons and were not drawn in order to have a better visibility of all components and signal traces. The ADC is at the border between analog and digital circuitry at the same height as the LC pi-filter which separates the analog from the digital VCC plane. The analog circuitry is placed as far away from potential sources of noise, the input of the power supply and the optical transmitters, as possible and all vulnerable signals are routed on the top layer. To increase the distance between the analog traces and the high speed digital signals (ADC data and CLK), the digital signals were routed on the bottom layer.
Parts of the PCB base material are removed underneath the connector for the voltage divider input and the resistors in order to increase the creepage distance and reduce potential creepage currents.
A large number of vias was placed along and inside the GND planes, and between high

speed signals to ensure that all grounds on all layers stay at the same potential, proper current return paths are provided and that crosstalk is minimized. Also, the ground impedance is reduced considerably this way and coupled or radiated EMI is expected have a reduced influence on signals and ground bounce therefore.
Pictures of the board's single layers with the GND planes drawn are given in the Appendix.

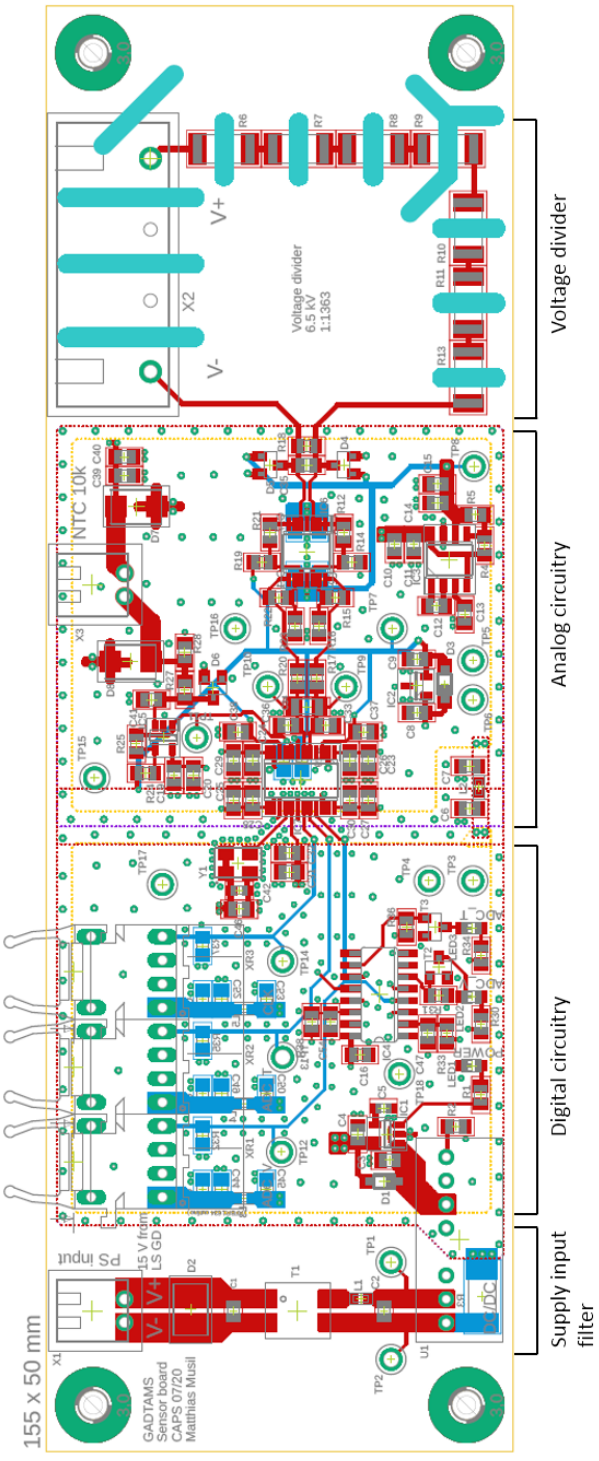


Figure 5.1: Sensor board PCB layout, red = layer 1, purple = layer 2, yellow = layer 3, blue = layer 4

5.3 Cell controller board

The layout of the cell controller PCB is given in Fig. 5.2. The GND planes are again indicated with dashed polygons and not drawn in this view. Refer to the Appendix for pictures of the single layers including the drawn planes. As for the sensor board, the supply input filter is locally separated from the rest of the circuit to avoid coupling effects. The connectors were arranged according to the current assembly plan for a switching cell. Also at this board the GND planes were stitched together properly with vias and attention was paid to proper spacing of high speed signal traces to avoid crosstalk. Due to space limitations, the decoupling capacitors for the FPGA supply pins were placed on the bottom layer, but an attempt was made to reduce parasitic inductance by placing them as close to their pins as possible and providing proper connecting traces. A number of vias was placed next to the FPGA IC's exposed pad to aid heat transfer to the GND plane and thus improve cooling. Pads were provided around the FPGA to allow the mounting of a metal shield if it is determined to be required.

Since the FPGA requires three different supply rails, VCCIO, VCCA and VCC_1, the

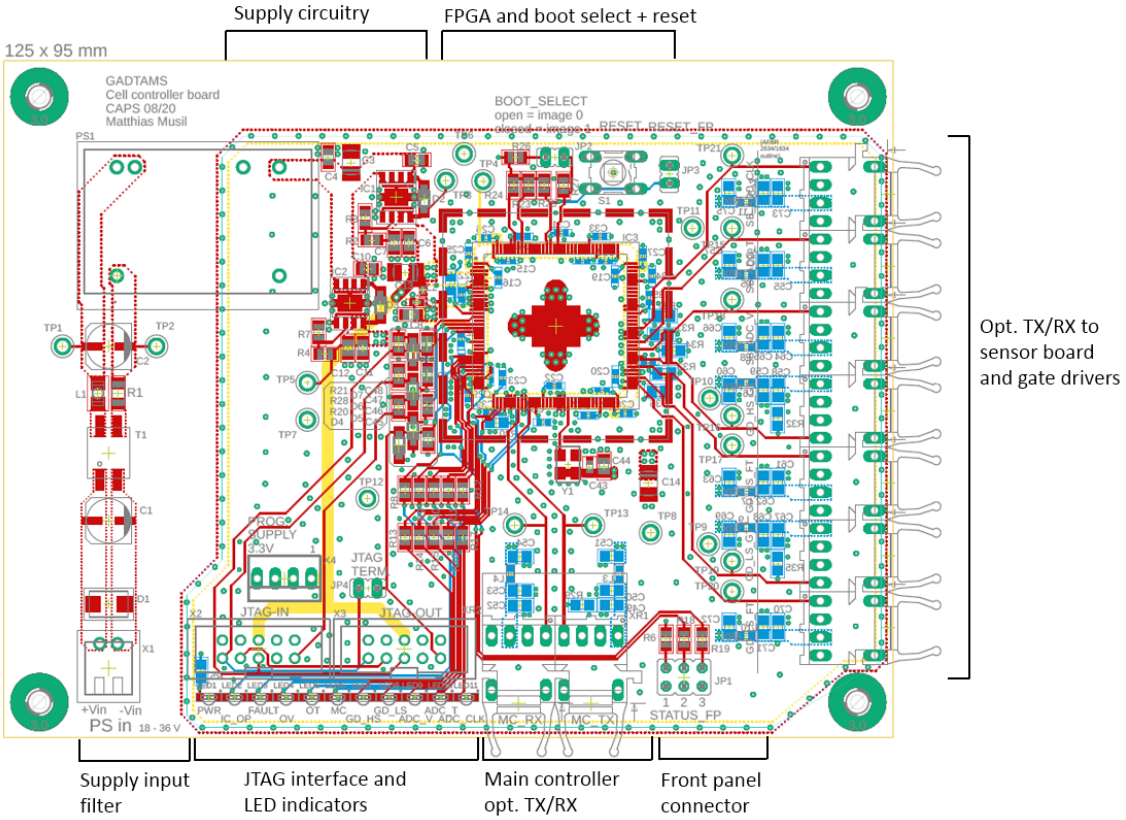


Figure 5.2: Cell controller board PCB layout, red = layer 1, purple = layer 2, yellow = layer 3, blue = layer 4

VCC plane needed to be split into three separate planes for each supply. Since the majority of the circuit is supplied by VCCIO, this planes spreads about the majority of the board. VCCA and VCC_1 are only needed by the FPGA, so they are limited to the area under the

IC. VCC_1 is spread in the free space under the chip package and VCCA in an interrupted ring under the FPGA's pins. The VCC planes are properly visible in the PCB layer pictures in the Appendix.

5.4 PCB Manufacturing

The PCBs were ordered for manufacturing and assembly with the following specifications:

- Layers: 4
- Min Trace/Space: 6 mil
- Min Hole size: 8 mil
- Thickness: 1.6 mm
- Solder Mask: Green
- Surface Finish: Immersion Gold
- Finished Copper: 1 oz
- Material Type: FR4
- Assembly of SMD components

Since the PCBs have not arrived yet at the time of writing this report, no pictures of the finished PCBs and thus no measurements or tests can be provided in the following. Work on this project will be continued though and all measurement and testing findings will be included in a later revision of this report.

6 Firmware and communication protocol

6.1 Firmware development and modules

At the time of writing this report, the firmware is still in development since it could not yet be programmed to the cell controller board and therefore be tested on hardware. It is structured into single modules with distinct functions which will be combined into a complete firmware after they individually passed testing. The modules are mostly developed using the Matlab Simulink HDL (hardware definition language) coder and pre-tested utilizing FPGA-in-the-loop-simulation (FIL simulation) on the previously selected DE0-Nano FPGA development board. Verilog code is exported with the HDL coder and used to eventually combine all modules using the intel Quartus FPGA development software. The firmware will have to be continuously developed further during and after the upcoming testing procedures including the prototype boards in order to fix any possible errors or adjust certain functions to newfound requirements or issues.
For a clear distinction to other communication protocols and for ease of documentation, the communication protocol developed in this project was given the working title 'Cell Controller Communication Protocol', or in short C3P.

The following modules are part of the FPGA firmware for the cell controller:

- ADC_Demodulator_Filter: As the name indicates, this module demodulates and filters the delta-sigma modulated bit stream from the sensor board's ADC.
- T_LUT: The temperature lookup table (LUT) is responsible for conversion of the demodulated voltage data from the temperature sensor into the corresponding temperature.
- C3P_CC_RX: This is the module responsible for receiving data (switching states and dead times) from the main controller on the cell controller side.
- C3P_CC_TX: This module is responsible for sending fault notifications from the cell to the main controller.
- Serial_TX: This module is planned to be an implementation of an asynchronous serial protocol, e.g. UART, which should be used to transfer voltage and temperature data in short packages to the main controller as long as no fault is present. Depending on how this works under EMI in operating conditions, the C3P might have to be extended to support transfer of this data. See section 6.4 for more information.
- PWM_Generator: Generates switching PWM signals for the gate drivers including the dead times specified by the MC.

- GDR_Fault_Handler: Listens for fault signals from gate drivers and handles reaction to fault.
- OV_OT_Handler: Checks for over voltage or over temperature and sets according status bits. If actions are determined to be required for OV or OT, they will be handled by this module.
- Status_Indicator: Turns on/off status LEDs depending on FPGA status.
- Cell_Controller_main: This is planned to be the top level module which initializes and manages all other modules. It should also include a state machine, for which the sates have to be defined based on which requirements are determined by the responsible for the main controller firmware and control.

The major modules, namely ADC_Demodulator_Filter, T_LUT, C3P_CC_RX, C3P_CC_TX, have been developed and pre-tested in the FIL simulation. Additionally, the main controller part of the C3P, which is an extension of the C3P_CC_TX, has also been developed within this project. The remaining modules are less complex than the already mentioned ones and will be developed in due time during testing of the prototype hardware.

The following sections will discuss the implementation of the mentioned major modules and show FIL simulation results.

6.2 ADC_Demodulator_Filter

6.2.1 Scope

As mentioned in section 4.2.2, the delta sigma ADC creates a bit stream of ones and zeroes at a rate of 10 MSps that correspond to the value of the measured voltage. This bit stream has to be demodulated and decimated to get a digital number with defined bit-width and reduced sampling rate which can then be used. A decimation filter was therefore developed using Matlab/Simulink with the intention to fulfill the specifications already listed in section 4.2.1. The following list includes previously defined and additional/modified filter specifications which arise from the design process:

- Output sampling rate: 19.53 kSps (10 MHz / 512)
- Measuring bandwidth (-0.1 dB): 5 kHz
- Resolution: >= 12 bit
- Filter output word length: 16 bit
- Filter coefficient word length: 14 bit
- Passband ripple: <0.01 dB
- Stop band frequency: 9.765 kHz
- Stop band attenuation: 80 dB

6.2.2 Filter design

The filter design presented below is a result out of an extensive literature review on digital filter design, [26, 29–38] and tutorials provided by the Matlab/Simulink documentation, [39–43]. It was decided to use a four-stage multi-rate decimation filter with a final decimation rate of 512. Such a filter architecture allows for a performance and space efficient implementation on the FPGA.

First, the required filter parameters, filter stages and their decimation ratios were defined. Then the single stage filters were designed using Matlab's DSP System Toolbox. The resulting digital filter coefficients are passed to a Simulink model of the filter which can be executed and tested in the FIL simulation and used to generate the Verilog HDL code.
The four stages of the filter with their decimation rates R are:

1. Sinc3 CIC (cascaded integrator comb) decimator with gain correction, R = 64
2. CIC compensation decimator, R = 2
3. Halfband decimator, R = 2
4. FIR (finite impulse response) decimator, R = 2

A block diagram of the filter is given in Fig. 6.1. It can also be seen that the results from the faster filter stages are provided as outputs too. These outputs are planned to eventually be used for fast over voltage detection.

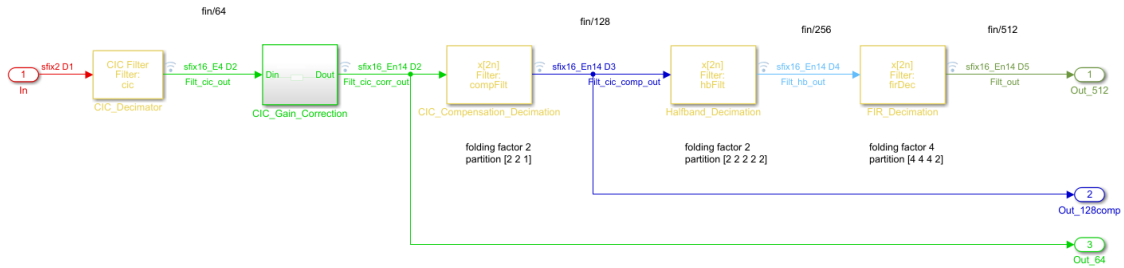
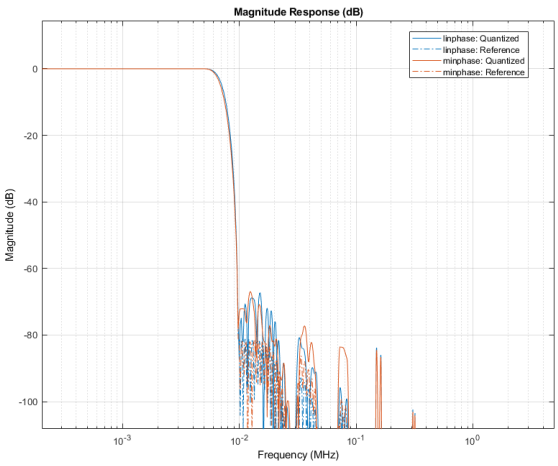


Figure 6.1: Simulink block diagram of the four-stage multi-rate decimation filter, i.e. the ADC_Demodulator_Filter module

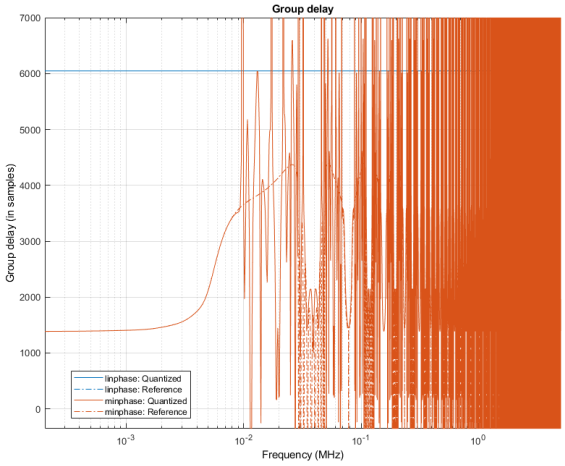
The Sinc3 CIC decimator efficiently decimates the input samples by a large factor of 64, with the only disadvantage that its transfer ratio is that of a sinc-curve, which causes a droop in the passband. As, among others, mentioned in [38], it also introduces a large gain of 18 bits or 262144 in numbers. It is therefore followed by a gain correction stage which reduces it to a number between 0 and 1.
The CIC compensation decimator's transfer ratio compensates the previous stage's passband droop and introduces a constant passband attenuation of 1, or 0 in decibels. Whilst doing so, it also reduces the sampling rate by a factor of 2.
The next stage is a halfband decimator, which is used to efficiently reduce the sampling

rate by another factor of 2. This filter is efficient because approximately half of its coefficients is zero, as the name suggests.
Finally, an FIR decimator sets the specified sampling rate down to 20 kHz. This is the most complex filter stage and has the task to ensure the total filter's specifications as given in the list at the beginning of this section.

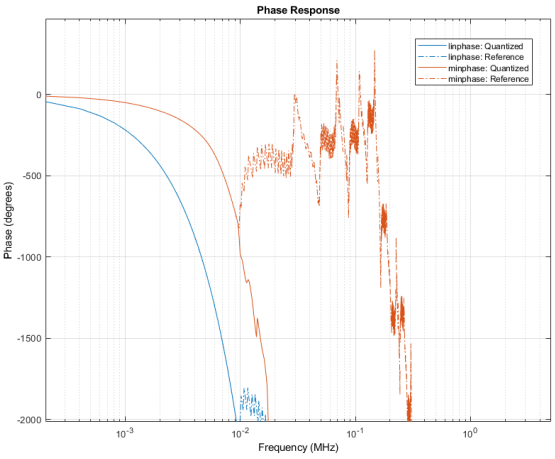
The filter design was then transferred into a fixed-point representation which is required



(a) Filter magnitude response



(c) Filter group delay



(b) Filter phase response

Figure 6.2: Filter magnitude & phase response and group delay vs. frequency for the linear and minimum phase designs of the reference (Matlab) and quantized (fixed-point) implementations

for the FPGA implementation. An output word length of 16 bit with a fraction of 14 bit is used for the filter data. The coefficients are defined with a word length of 14 bit and a fraction of 13 bit. These fixed-point representations are still subject to change if it is determined that a different combination of word and fraction lengths yields better results.

The filter was implemented once in a linear phase and once in a minimum phase design. The difference is, that a linear phase filter has a constant group delay, i.e. delay in samples

it takes from the data input to a data output, over the whole frequency range, while a minimum phase filter has the lowest possible group delay which varies across the frequency range though. Linear phase filters are important in audio or frequency measurement applications, where the signal's spectrum should not be distorted. In this application, this is not a requirement though and speed is more a priority. Therefore the minimum phase design was chosen for this filter. The magnitude & phase response, and the group delay of both implementations are given in Fig. 6.2. It also includes a comparison between the reference from Matlab and the quantized version using the fixed-point representation mentioned above.
It can be seen that the filter specifications are generally fulfilled. However, the quantized version's stopband attenuation is less than 80 dB which means that additional tweaking of the fixed-point parameters will be required. Other than that, the linear and minimum phase design have very similar magnitude responses. A big difference can be seen in the phase response. The linear phase filter has a significantly higher phase shift than the minimum phase design. Also, at frequencies beyond the stop band, the quantized version of the minimum phase filter behaves very differently from the reference, which is not an issue though as any frequencies in this range are basically attenuated completely anyway. The filter group delay graph shows that the minimum phase filter's phase response is almost constant in the passband frequency range up to 5 kHz and lower than the linear phase filters group delay by a factor of almost 6. This directly translates into a filter output which is 6 times faster.

6.2.3 FIL simulation

The final filter design was then converted into HDL code and tested in a FIL simulation. Fig. 6.3 shows the block diagram including the Simulink reference (blue) and the FIL block. The design is tested with a test signal generated in Matlab. It has a DC voltage of 4 V and ripple of 0.4 V with a frequency of 2 kHz. A voltage transient with a rise time of 14.74 kV/s, which can be expected at the ADC input, is also included in order to test the transient response of the filter. The test signal is modulated into a bit stream with a simulated delta-sigma function and then fed to the demodulator filter in Simulink.

The FIL simulation result is given in Fig. 6.4. It can be seen that the FIL output of the filter (filt_fil) resembles the input signal at a reduced sampling rate. Also, the peak of the transient is not completely caught due to the filter's bandwidth limitation. The filter delay is measured by the delay from the peak in the input signal to the peak on the filter output. It is around 340 μs, which is below one period of the 2 kHz signal and therefore suitable for indication of the cell capacitor voltage and control purposes. For detection of overvoltages, this is too slow though. The faster outputs (64 and 128comp) are delayed by around 180 μs which is better but also not yet completely satisfactory. More work has to be put into the design of this filter to improve its delay and make it faster.

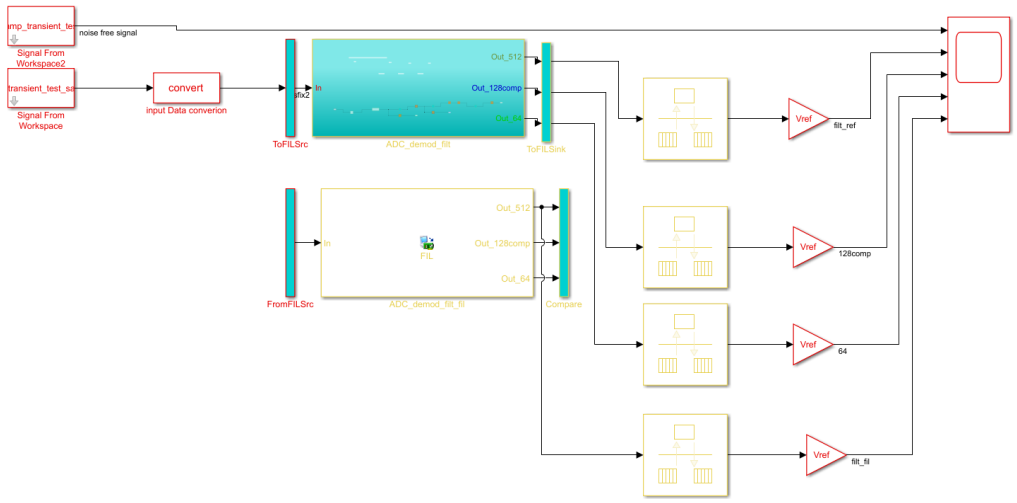


Figure 6.3: Simulink block diagram of the digital filter in the FIL simulation

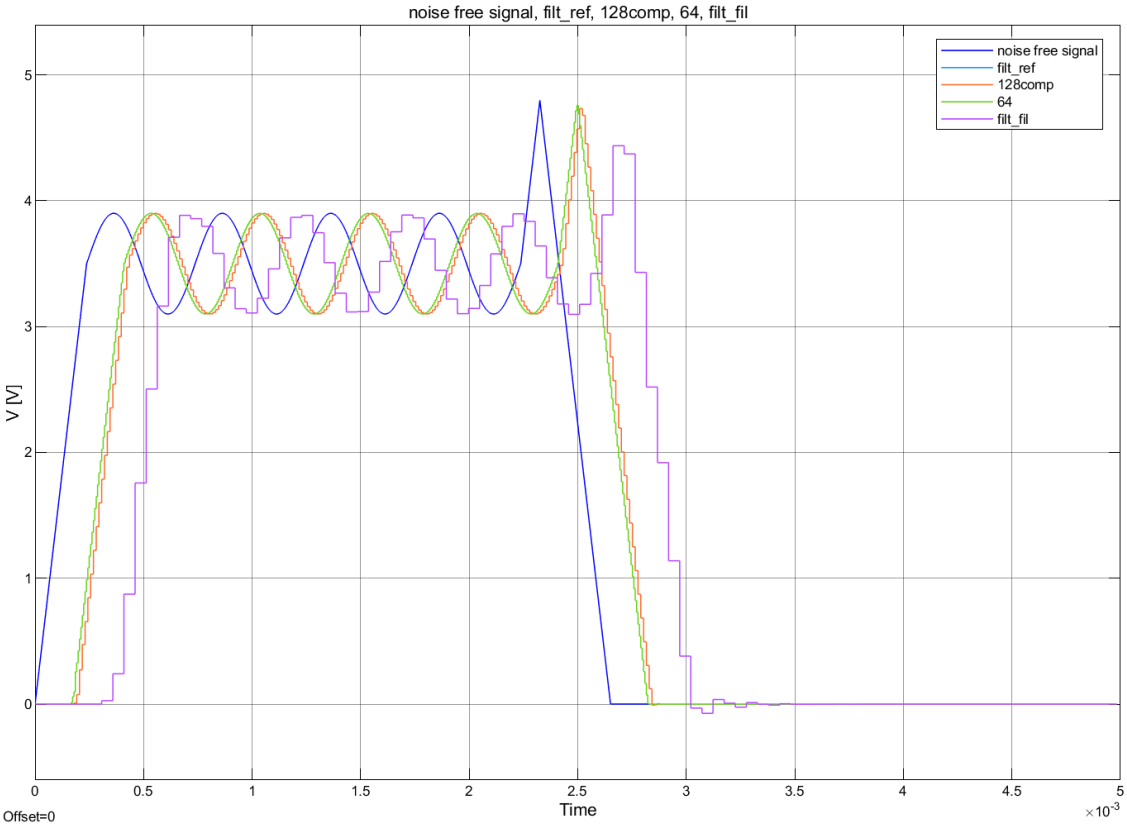


Figure 6.4: FIL simulation output of the digital filter

6.3 T_LUT

6.3.1 Scope and implementation

In order to retrieve the measured temperature value from the measurement circuit discussed in section 4.2.5, a one-dimensional lookup table (1-D LUT) was implemented. The lookup table contains the voltages and temperatures from the curve in Fig. 4.6(b) as breakpoints and table data respectively. However, not the real voltages between 0 and 5 V are passed to the table, but the relative values between 0 and 1 which are output by the digital filter. This way, a multiplication operation (with the ADC reference voltage) can be avoided and the further design of the LUT is simplified. Since the LUT has to be implemented discretely for the FPGA with a reasonable size, 60 points of the curve were stored to the table. HDL implementation of the LUT is most efficient if evenly spaced points are used, therefore the voltage breakpoints are spaced with a dV of 2^{-6} which, as a multiple of $2^{-}1$, guarantees equal spacing also in fixed-point presentation, as it is required by the FPGA. The temperature table data is then calculated from these voltage breakpoints and also converted to fixed-point presentation.
A word length of 16 bit with a fraction of 14 bit is used for the voltage breakpoints, which corresponds to the digital filter's output word length. The temperature data is stored also with 16 bit word length but a fraction of 7 bit. This was chosen since at least 8 bit are required to represent temperatures up to $160°C$ and the fractional accuracy is not important. It is required though that input and output of the LUT share the same total word length.
The LUT is configured as follows:

- Interpolation method: Linear point-slope
- Extrapolation method: Clip
- Index search method: Evenly spaced points

The interpolation method determines how inputs between the stored breakpoints are treated. Here, the stored curve is interpolated linearly to return a value between breakpoints. When an input value exceeds the last breakpoint, the output is clipped to the last data point in the table. The specified search method is very fast for this LUT implementation, since multiples of 2 are used for the breakpoint spacing. This way, the search is done by a simple bit shift operation.

The implementation of the T_LUT is given in Fig. 6.5. To avoid errors in the LUT, the input voltage data is first checked. If it is below the minimum or above the maximum table data, Vmin is fed to the LUT to avoid execution issues. Additionally, the OUT_VALID output goes to 0, which notifies all modules which use the temperature output of the error.

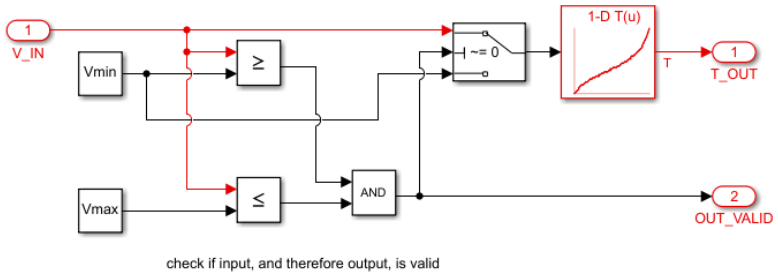


Figure 6.5: Block diagram of the LUT implementation

6.3.2 FIL simulation

The LUT implementation was tested in an FIL simulation by feeding 1701 different voltages between 0.04 and 0.96 (i.e. 0.2 and 4.8 V) to the LUT on the FPGA. The temperature outputs where then fed back to Matlab to calculate the error between the expected and reference values which arises from the linear interpolation. As can be seen in Fig. 6.6, the error at the linear range from around 20 to 80 °C is basically zero. This was expected as linear interpolation is used by the LUT. In the nonlinear regions, also the error increases nonlinearly. The largest error of 0.58 K is observed at around 155 °C which is negligibly small at this high temperature. Generally, accuracy is not a big issue for the temperature measurement and especially in the main operating temperature range from 20 to 100 °C the error due to the LUT is far below 0.1 K.

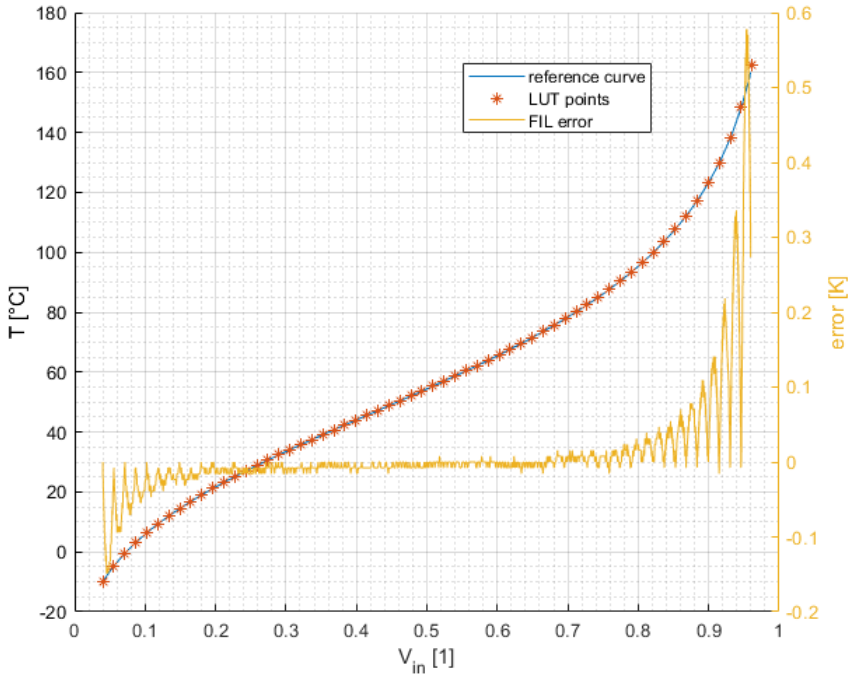


Figure 6.6: FIL simulation result for the T_LUT module

6.4 Cell Controller Communication Protocol (C3P)

6.4.1 Scope

This communication protocol should be used for an efficient and safe communication between the main controller and a cell controller over two optical fibers. It allows the main controller to send switching states and fault signals to the cell controller. Also, the switching dead time should be adjustable via this protocol. The cell controller can transmit fault signals through this protocol and, as an initial plan, be able to transmit measurement data via an integrated SCI (serial communication interface) such as UART. As mentioned before, if serial data transmission via an SCI does not work under EMI in operating conditions, the C3P will have to be extended to support this data transfer. The protocol's bus encoding allows for a quick detection of fault signals and link faults, and is expected to provide resilience against heavy EMI.

6.4.2 Principle and definitions

The principle of this communication protocol is to encode the information into clearly distinguishable states of frequency and duty cycle. The required bus encoder, or transmitter, is basically an improved PWM generator and the receiver can be implemented as a frequency counter. The expected advantages of this communication protocol are:

- A robust, error free transfer of switching states, dead time settings and fault signals
- Automatic and fast detection of link failures and fault signals
- Bidirectional transfer of data via only 2 fibers with no need for synchronization

Figures 6.7 and 6.8 show the signal states of the protocol under normal and fault conditions respectively, which should illustrate the principle explained above. The variables given in the figures are defined in table 6.1.
The main controller will generate a PWM signal in a control loop. This PWM signal represents the switching states of the half-bridge. A rising edge means a transition from 01 (upper switch off, lower switch on) to 10 (upper switch on, lower switch off) and a falling edge from 10 to 01. The main controller encodes this PWM signal into the required signal states. Frequency f_2 (5 MHz) at a 50 % duty cycle d tells the cell controller to keep the current switching state. Additionally, 5 more duty cycles with increments of 15 % are available at f_2 to adjust the dead time during operation. Frequency f_1 (10 MHz) with duty cycle d_1 (80%) indicates a rising edge, while f_1 with d_2 (20%) indicates a falling edge. The cell controller requires 1 period of f_1, times T_r and T_f, to recognize the command and send the gate driver control signals accordingly. An adjustable dead time T_{dt} is added in order to avoid short-circuiting the half bridge. While the main controller communicates the required switching sates via the downstream fiber, the cell controller transmits the voltage and temperature data on the upstream fiber.

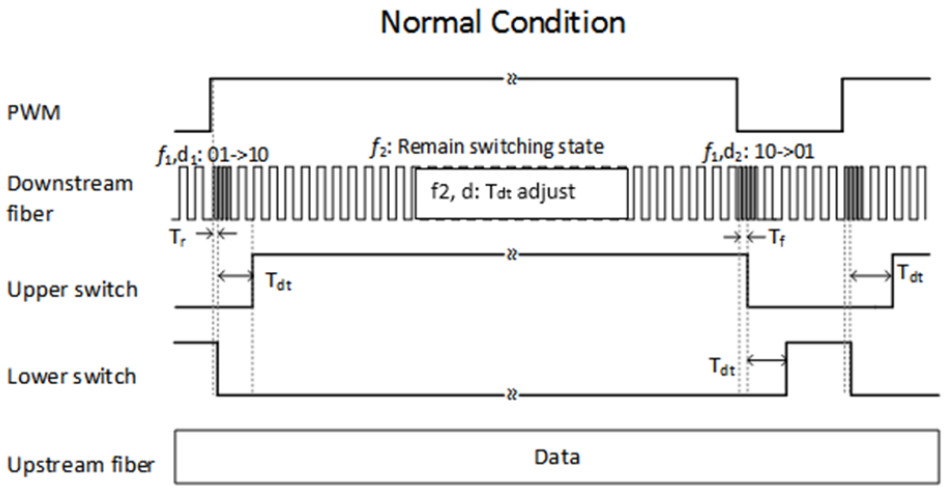


Figure 6.7: C3P signal states under normal operating conditions

A fault, e.g. a false triggering, is generally detected by the gate drivers which then notify the cell controller. The controller consequently enters a fault state where it turns off both switches of the half bridge and sends the fault signal to the main controller on the upstream fiber. The fault signal is characterized by f_1 with $d_3 = 50$ %. This will be picked up by the main controller within 1 period of f_1, i.e. 100 ns, after which it will immediately react to the fault. The current strategy is for it to put out the same fault signal to all other cell controllers of the MMC. This signal is then picked up by the remaining cell controllers which will also turn off their switches to bring the MMC into a safe state. The fault state can then be cleared by putting out the f_2, d signal. For now it is planned to

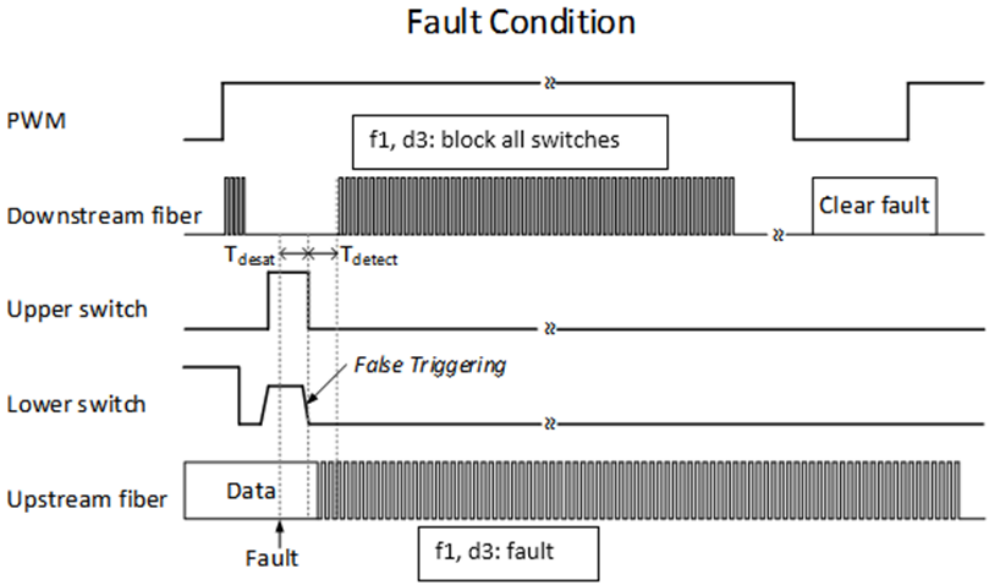


Figure 6.8: C3P signal states under fault conditions

use an SCI for the upstream data. The data should be in 24 bit data packets. The first 8

bit should include an ID which identifies the switching cell and data, and the other 16 bit should include the data word.

Table 6.1: Definitions of design variables

Variable	Definition	Value	Location
f1, d1	Rising edge	10MHz, 80% duty	Optical fiber RX
f1, d2	Falling edge	10MHz, 20% duty	Optical fiber RX
f1, d3	Fault, Block all switches	10MHz, 50% duty	Optical fiber TX/RX
f2	Remain switching state, No f2 means to block (link failure)	5MHz, 50% duty	Optical fiber RX
f2, d	Deadtime adjustment via duty cycle increments of 15 %	5MHz, 5 duty cycles available	Optical fiber RX
Tr	Turn on delay, caused by latency	100ns	Cell controller
Tf	Turn off delay, caused by latency	100ns	Cell controller
Tdt	Deadtime, adjustable via f3, d	200ns-1us adjustable	Cell controller
Tdesat	De-sat protection time	TBD	Cell controller
Tdetect	Fault detection time	100ns	Main controller
DataV	Cell + data ID + Cell Voltage	1x 8bits SCI f. ID	Optical fiber TX
		2x 8bits SCI f. data word	
DataT	Cell + data ID + Cell Temperature	1x 8bits SCI f. ID	Optical fiber TX
	reduced data rate	2x 8bits SCI f. data word	

6.4.3 Implementation

This section will discuss the implementation of the transmitter and receiver parts of the cell controller communication protocol. The transmitter module discussed here is the full implementation which will run on the main controller. The cell controller module C3P_CC_TX will be a reduced version of this, since it only needs to transfer the fault state. The receiver module will be implemented in the presented form at the main and cell controller.

6.4.3.1 Transmitter

The Simulink implementation of the transmitter module is given in Fig 6.9. The module will run at a clock of at least 100 MHz, which is required to generate the specified signal states and duty cycles with enough accuracy. Inputs are 'FAULT_FLAG_IN', 'PWM_CODE_IN' and 'DT_SELECT', which are the fault flag, PWM signal from the control loop and selected duty cycle respectively. The output 'TX_OUT' is the frequency/duty cycle encoded signal. The two counters CNT10 and CNT5 count from 0 to defined maximum values, then reset and start again, which creates staircase signals with frequencies of 10 and 5 MHz respectively. The PWM10_DC_Adjust block then creates the 10 MHz (f_1) PWM signal (PWM10) with the currently required duty cycle based on the states of the fault flag and PWM code. Per default, the 5 MHz, 50 % duty cycle (f_2, d) signal (PWM5) is output. If the dead time should be adjusted, the duty cycle of f_2 is changed accordingly. The PWM10_Enable block controls the transition from PWM5 to PWM10 at the output, such that the optimal performance is achieved. The transition is initiated with a single tick of 'low', i.e. 0 V, and followed by 4 periods of the PWM10 signal. At the end of the last PWM10 period, the output signal smoothly transitions back to PWM5. This way, the switching states and fault signals are transmitted immediately as they occur with a clear distinction to the PWM5 signal. The total delay until the receiver recognizes the signal is then 100 ns + 1 tick of the transmitter clock, which is 10 ns here, so 110 ns. The, possibly, distorted last PWM5 period before the transition to PWM10 will be simply discarded by the receiver as it will not fit into any know combination of frequency and duty cycle.

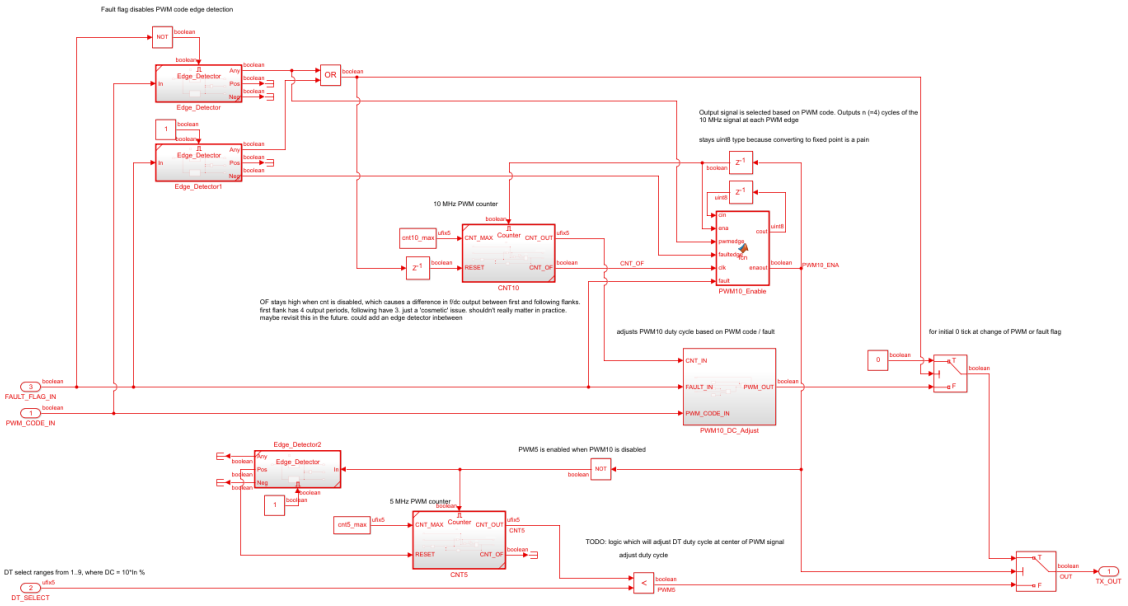


Figure 6.9: Simulink block diagram of the C3P transmitter module

6.4.3.2 Receiver

The Simulink block diagram of the receiver module is given in Fig. 6.10. It basically consists of an improved frequency counter, which is named D_P_Counter to reflect that it counts the number of receiver clock (200 MHz) ticks that fit into a whole period of the received signal 'RX_IN', 'PERIOD_CNT', and the number of ticks during which the received signal is high, which represents also its duty cycle and is thus called 'DUTY_CNT'. The 'VALID' output is used to signal whether an output is valid and can be used for further processing. As it can be seen, this output is used to enable the state lookup table which links the counted period and duty ticks to a certain signal state. The 'STATE_OUT' output can then be used by the firmware's main module to initiate the required actions, like switching the HB module, entering a fault state or changing the dead time. The other outputs of the module are currently used for debugging purposes.
The lookup table is given in Fig. 6.11 and the corresponding signal states are described in table 6.2. The duty (d) and pulse (p) counts in the figure correspond to the frequencies and duty cycles defined in table 6.2. All zeros in the LUT refer to an invalid input and will simply be discarded by the receiver. If too many invalid inputs occur after each other, it is planned to enter a fault state in order to resolve the apparent issue. The black boxes around the defined states indicate a 1 tick tolerance which will be implemented and tested with the prototype boards. The main idea behind it is to compensate for asynchronism between main and cell controller. Depending on how this works during testing, the tolerance will be removed or increased. At the current implementation, there are always at least 3 ticks of difference between defined signal states which is expected to be sufficient for EMI robustness of the protocol.

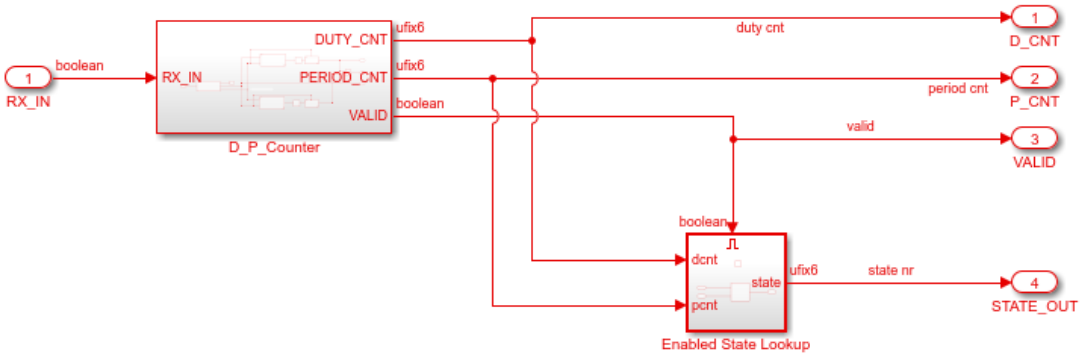
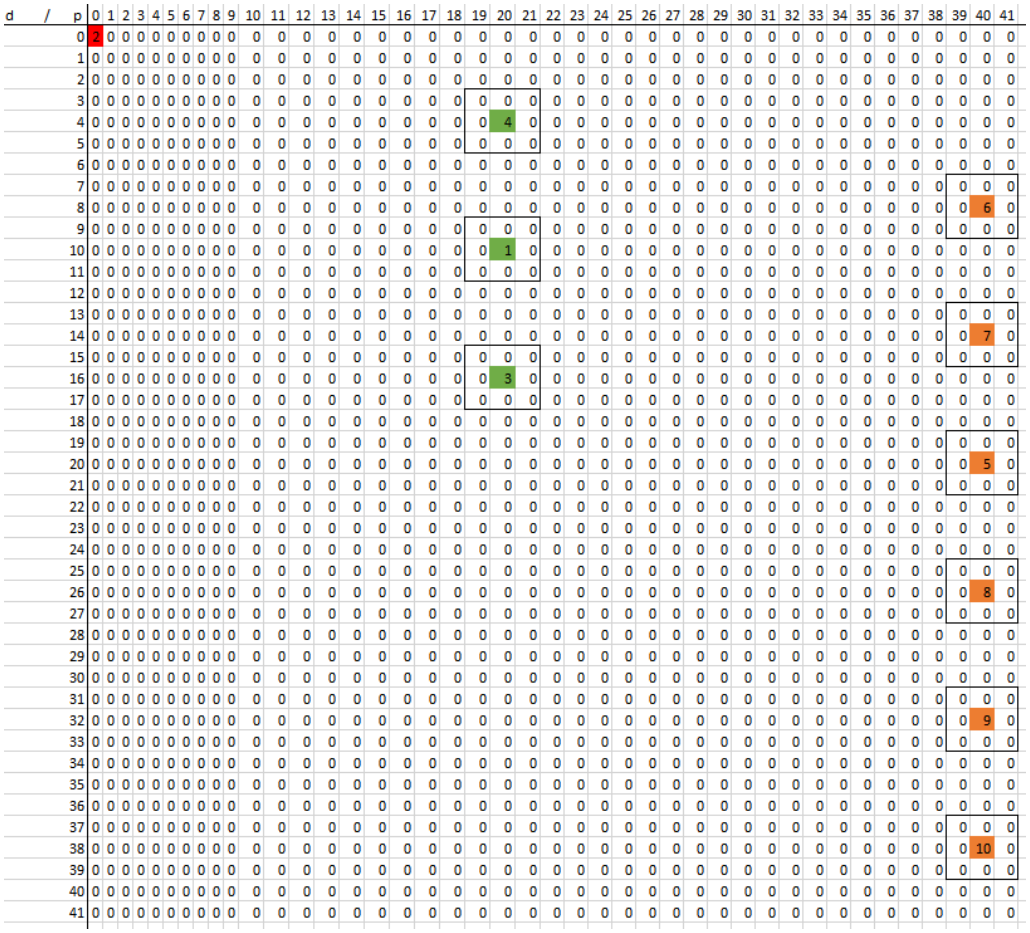


Figure 6.10: Simulink block diagram of the C3P receiver module



d / p	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41
0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	0
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	0
27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	9	0
33	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	0
39	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.11: Lookup table for the C3P_CC_RX frequency and duty cycle counter states considering a 200 MHz clock

Table 6.2: Currently defined signal states and corresponding cell controller actions

State Nr.	f [MHz]	DC [%]	Description	Action
1	10	50	f1, d3, fault	switch off US and LS
2	-	-	only zero input, link failure	switch off US and LS
3	10	80	f1,d1, rising edge	switch off LS, wait DT, switch on US
4	10	20	f1,d2, falling edge	switch off US, wait DT, switch on LS
5	5	50	f2, keep current state	do nothing
6	5	20	f2, change DT	adjust DT
7	5	35	f2, change DT	adjust DT
8	5	65	f2, change DT	adjust DT
9	5	80	f2, change DT	adjust DT
10	5	95	f2, change DT	adjust DT
0	else	else	zero state/invalid input	do nothing

The implementation of the D_P_Counter block is given in Fig. 6.12. An edge detector determines the input signal's current edge, positive or negative. At a positive edge, the counter 'CNTH' is started. Analogously, at a negative edge the counter 'CNTL' is started. The counters operate at the receiver clock of 200 MHz. Simultaneously, a positive edge resets 'CNTL' and causes its last output to be held. A negative edge does the same to 'CNTH'. The 'CNTH' output is the duty count and the sum of 'CNTH' and 'CNTL' is the period count. The outputs of the block are always valid at the next positive edge of the input signal.

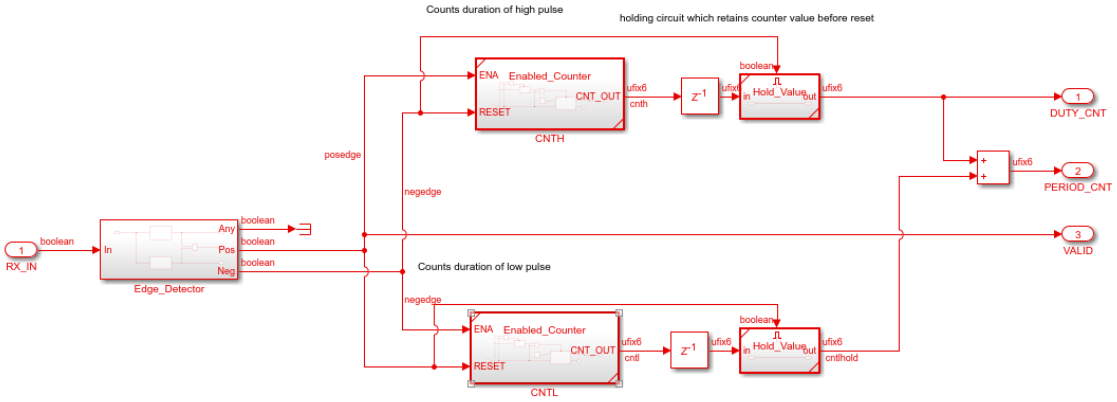


Figure 6.12: Simulink block diagram of the D_P_Counter block

6.4.4 Simulation

The protocol has been tested in a regular Simulink simulation so far, since a proper FIL simulation would require two FPGAs which are not available at this point of time. This test will be done when the prototype boards arrive and thus enough hardware is available. In the simulation of the protocol, test signals (PWM code, duty cycle adjust and fault) are generated and fed to the transmitter module. The transmitter's output is then fed to the receiver module's input. The test is successful if the receiver puts out the correct signal states at the end.

6.4.4.1 Normal operation

For the normal operation, a test PWM code and all possible PWM5 duty cycles are fed to the transmitter module. Fig. 6.13 shows the result of the simulation. It includes the PWM code, the transmitter signal TX (not visible in this view as it is a very fast signal), from the receiver module the duty and period count values, the valid indicator and the resulting recognized states. It can be seen that the duty counter correctly counts all possible duty cycle steps. The receiver correctly recognizes which duty counts are valid signal states and puts out the correct state numbers, refer to table 6.2. Also the positive and negative edge of the PWM code are correctly transmitted and received, as it can be seen by the '3' and '4' states at the state number graph at the same times as the PWM edges. Fig. 6.14

includes the zoomed view of the PWM code's positive edge. It can be seen how the output signal transitions from PWM5 to PWM10 and that the state is then correctly recognized by the receiver after a full cycle.

6.4.4.2 Fault condition

Similarly, a test was done for the fault condition. The same PWM code as before was used, but it is interceded by a fault flag for a certain amount of time. As can be seen in Fig. 6.15, the fault state '1' is correctly detected at the receiver side, also no switching signal '3' or '4' is detected during the fault. The fault signaling therefore works as expected. Fig. 6.16 shows the zoomed view of the fault signals positive edge. It can be seen how the TX output transitions to the fault signal state and how it is correctly detected at the receiver after one period.

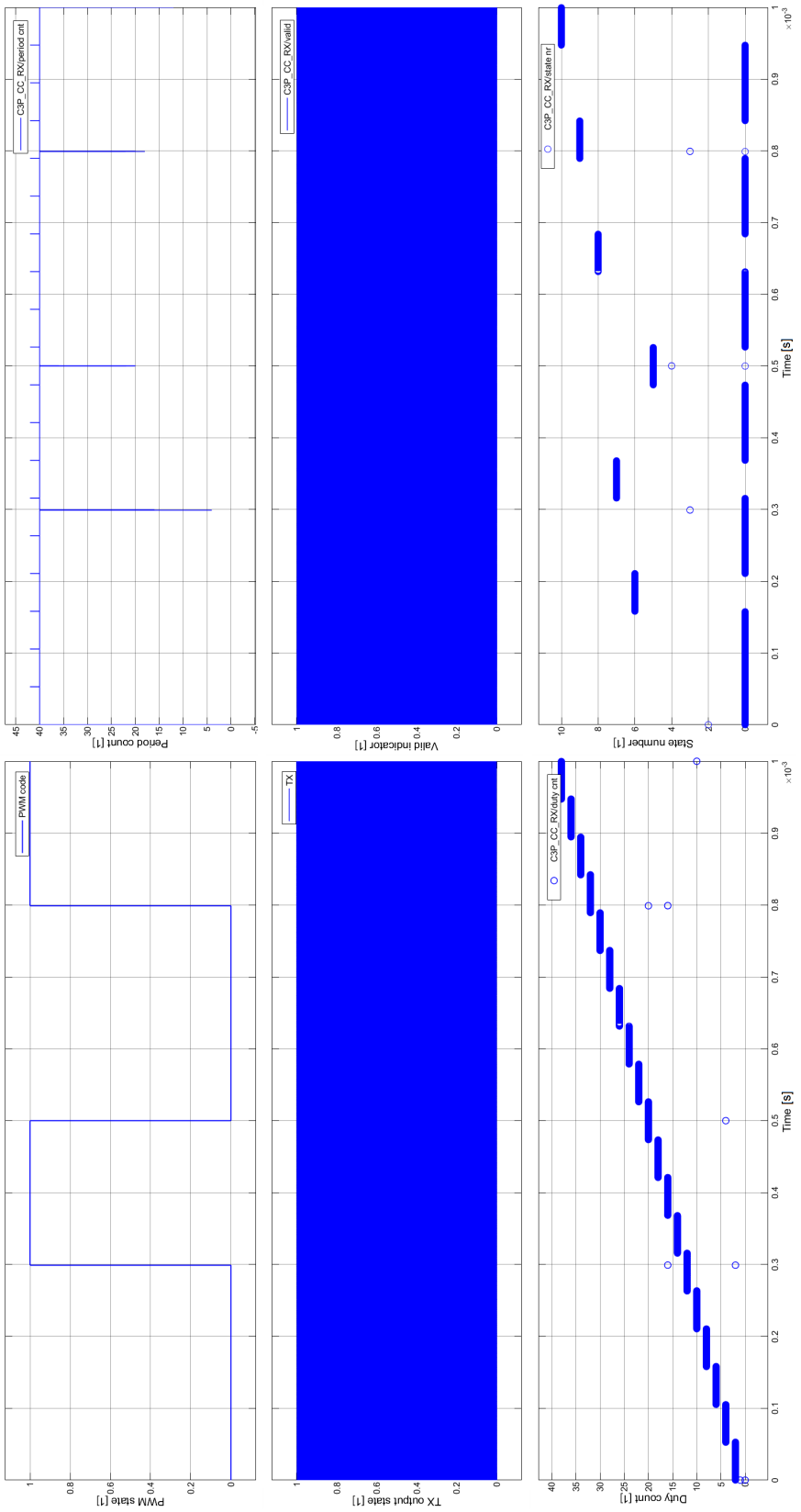


Figure 6.13: Simulation output of the transmitter/receiver chain under normal operation

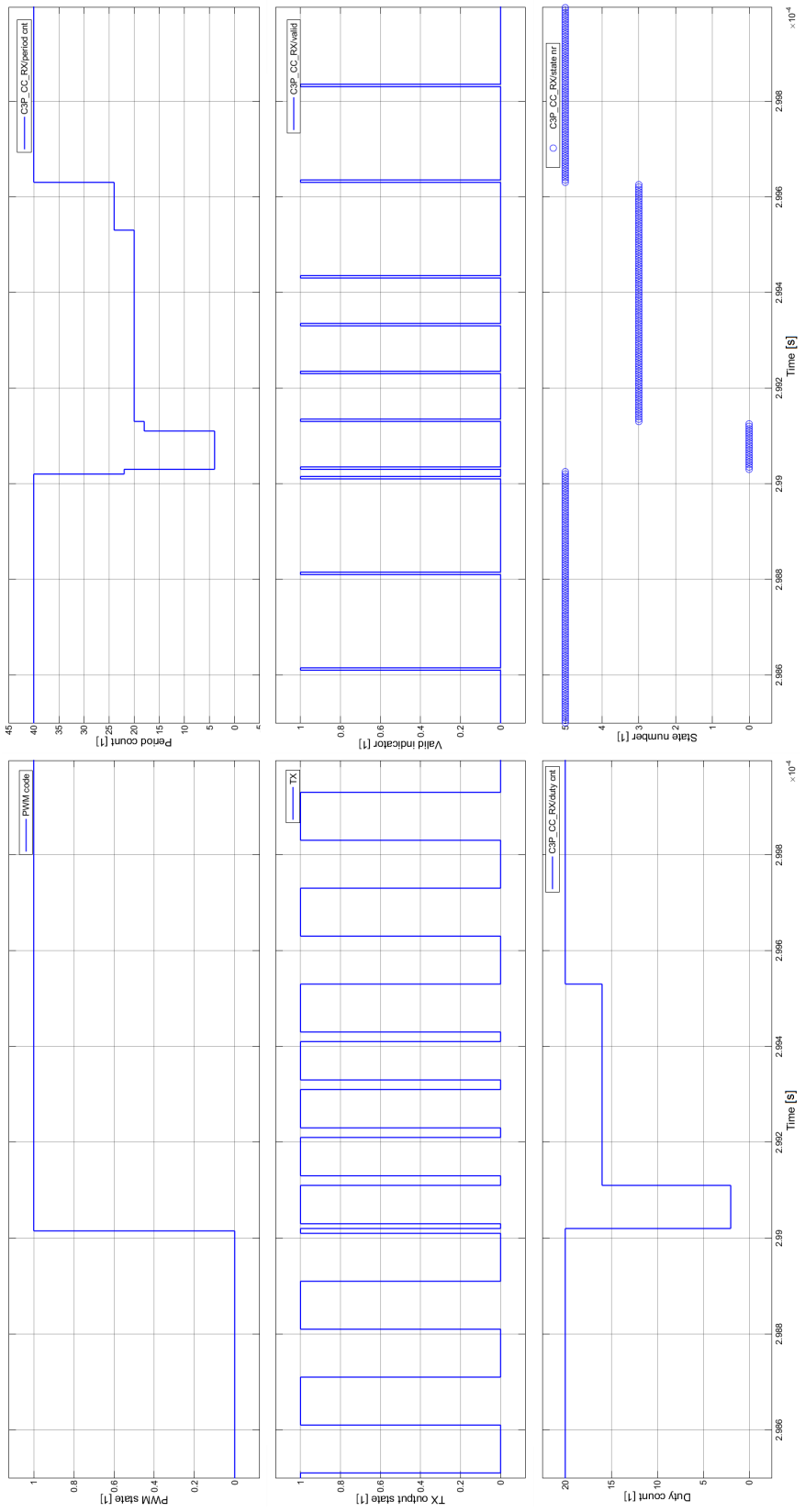


Figure 6.14: Simulation output of the transmitter/receiver chain under normal operation, zoomed view of PWM positive edge

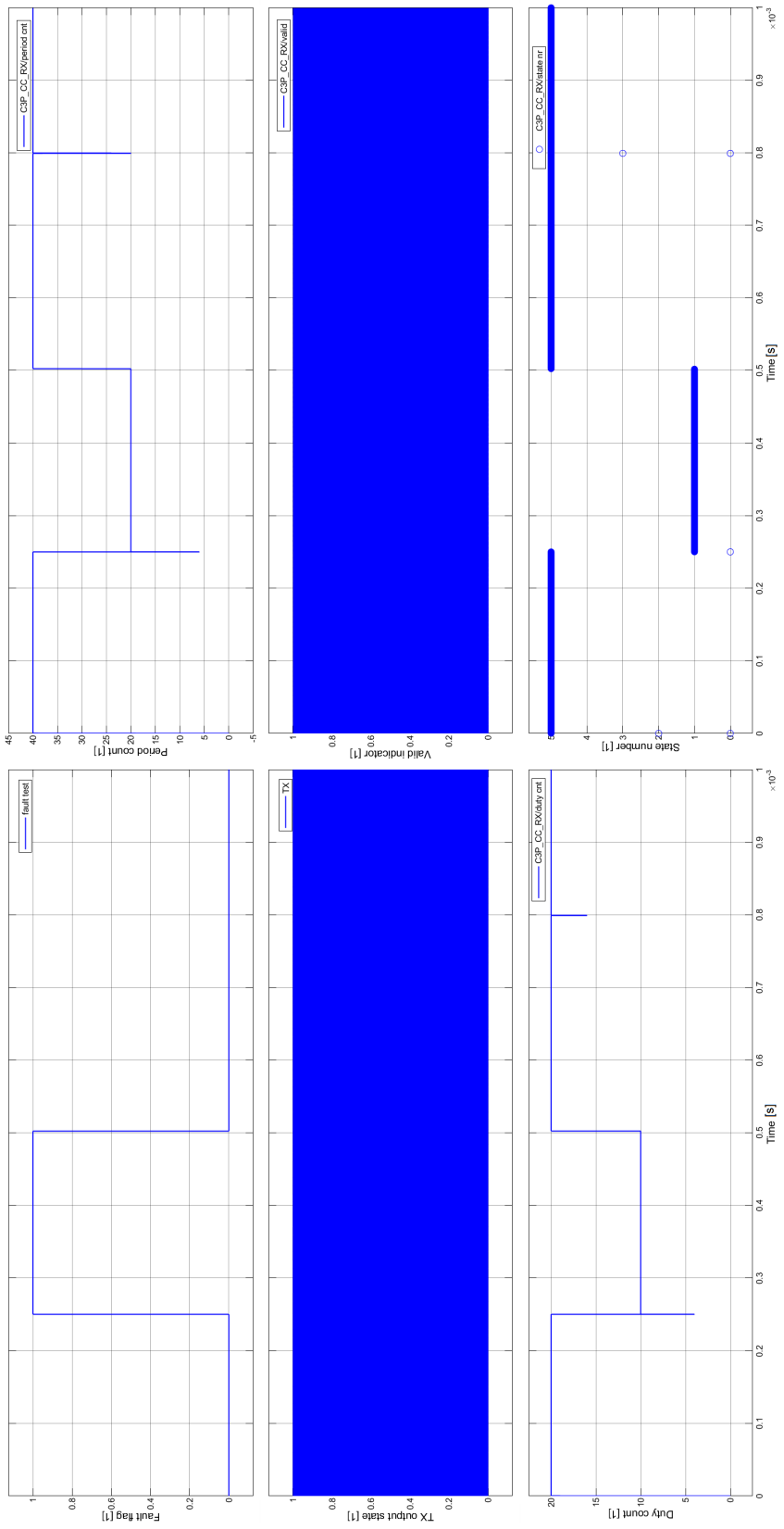


Figure 6.15: Simulation output of the transmitter/receiver chain under fault conditions

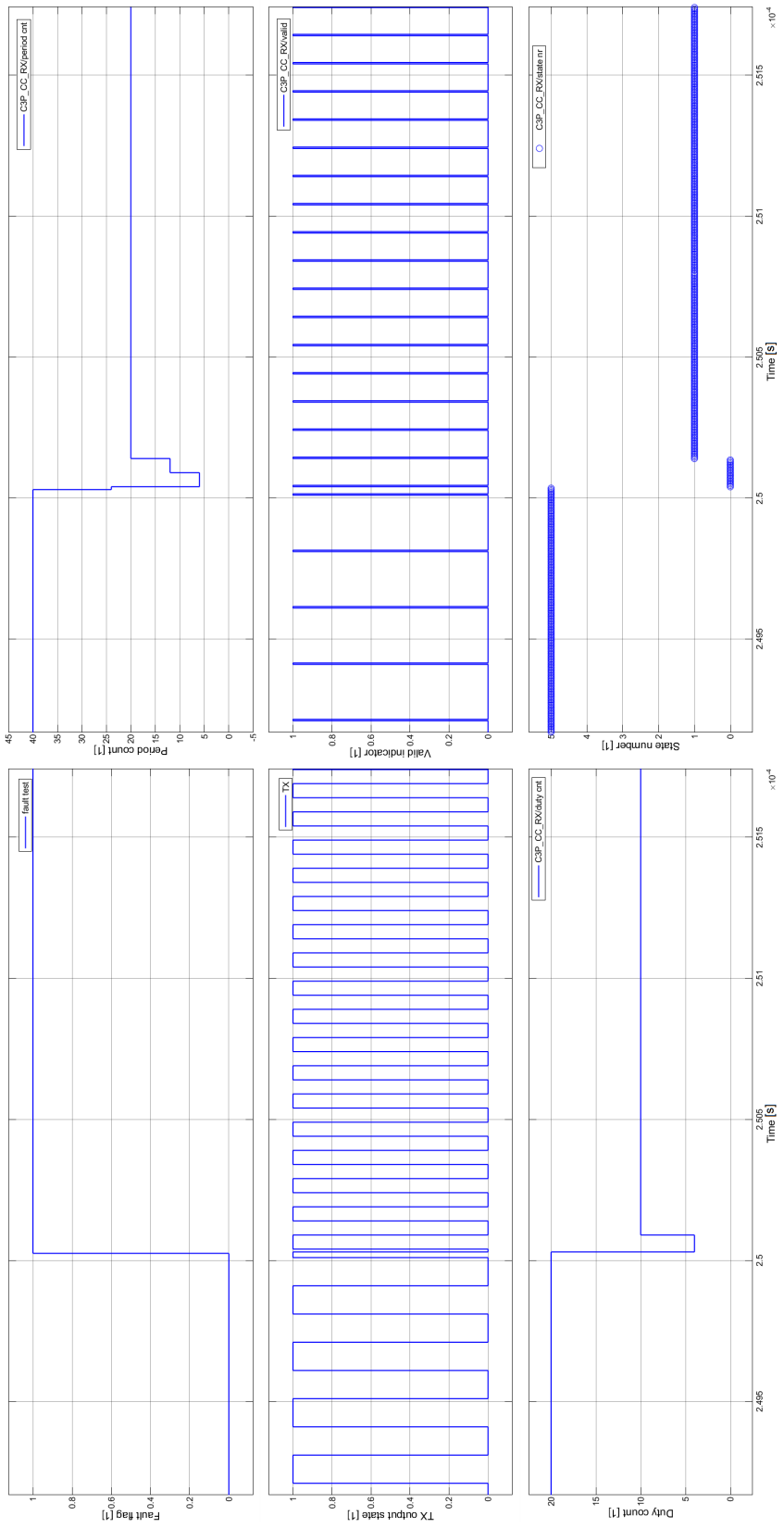


Figure 6.16: Simulation output of the transmitter/receiver chain under fault conditions, zoomed view of positive edge on fault flag

6.4.4.3 Conclusion

The conclusion of the simulation test of the communication protocol is, that so far it works as specified and expected. Further testing has do be done on hardware and under influence of EMI in order to verify whether it actually works and fulfills all specifications and requirements.

7 Conclusion

7.1 Summary

The aim of this project was to develop a cell controller for a switched capacitor modular multilevel converter which is able to operate under heavy EMI caused by the fast switching of SiC HB modules. The development should be based on a literature review on WBG devices and simulation tools.

First, the specifications and requirements for the cell controller were determined and fixed as base for the design process. A literature review was done which showed the importance of EMI control strategies in applications using WBG devices. Some mitigation strategies were summarized and considered for the design of the circuit and PCB. It was determined to split the cell controller into a controller and a sensor board for improved EMI robustness. A circuit concept was developed and realized for both boards and their implementation was thoroughly discussed. PCB prototype designs have been created and ordered for manufacturing. Then the firmware, including a digital demodulation filter and a communication protocol were developed using Simulink and FIL simulations.

At this point of time, the PCB prototypes have not yet arrived and could not be tested. The parts of the firmware which are implemented already were tested successfully using FIL simulations. For this reason, it can not yet be concluded that the cell controller developed in this project fulfils all requirements and is able to operate under influence of heavy EMI.

7.2 Outlook

Work on this project will be continued until the hardware has been tested successfully, first under lab and eventually in actual operating conditions. A measurement and testing plan are currently being developed in order to test the hardware as soon as it arrives. Further work on the firmware is being conducted in order to finalize the FPGA design. In order to be able to test for all probable faults, a failure mode and effects analysis (FMEA) is also being performed and is expected to provide valuable insights to the design of cell controllers for MMCs using WBG devices.

The interested reader is invited to contact the author about updates on the progress of work and the final version of the Master's thesis which this report will eventually be formed into.

8 List of figures

9 List of tables

10 Bibliography

[1] Boyi Zhang and Shuo Wang. A Survey of EMI Research in Power Electronics Systems with Wide-Bandgap Semiconductor Devices. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(1):626–643, 2020.

[2] Yue Xie, Cai Chen, Zhizhao Huang, Teng Liu, Yong Kang, and Fang Luo. High Frequency Conducted EMI Investigation on Packaging and Modulation for a SiC-Based High Frequency Converter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(3):1789–1804, 2019.

[3] Murata. Text No. TE04EA-1; Differential and Common Mode Noise. pages 26–30.

[4] Yingjie Zhang, Shuo Wang, and Yongbin Chu. Comparison of radiated electromagnetic interference (EMI) generated by power converters with silicon MOSFETs and GaN HEMTs. *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2019-March(1):1375–1382, 2019.

[5] Ivan Josifović, Jelena Popović-Gerber, and Jan Abraham Ferreira. Improving SiC JFET switching behavior under influence of circuit parasitics. *IEEE Transactions on Power Electronics*, 27(8):3843–3854, 2012.

[6] Niall Oswald, Philip Anthony, Neville McNeill, and Bernard H. Stark. An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched All-Si, Si-SiC, and All-SiC device combinations. *IEEE Transactions on Power Electronics*, 29(5):2393–2407, 2014.

[7] Andrew Trentin, Liliana De Lillo, Lee Empringham, Pat Wheeler, and Jon Clare. Experimental comparison of a direct matrix converter using Si IGBT and SiC MOSFETs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 3(2):542–554, 2015.

[8] Bingyao Sun, Rolando Burgos, and Dushan Boroyevich. Common-Mode EMI Unterminated Behavioral Model of Wide-Bandgap-Based Power Converters Operating at High Switching Frequency. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(4):2561–2570, 2019.

[9] Di Han, Silong Li, Yujiang Wu, Wooyoung Choi, and Bulent Sarlioglu. Comparative Analysis on Conducted CM EMI Emission of Motor Drives: WBG Versus Si Devices. *IEEE Transactions on Industrial Electronics*, 64(10):8353–8363, 2017.

[10] Di Han, Casey T. Morris, Woongkul Lee, and Bulent Sarlioglu. A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs. *IEEE Transactions on Transportation Electrification*, 3(1):168–179, 2017.

[11] Krishna Mainali and Ramesh Oruganti. Conducted EMI mitigation techniques for switch-mode power converters: A survey. *IEEE Transactions on Power Electronics*, 25(9):2344–2356, 2010.

[12] Alejandro Paredes Camacho, Vicent Sala, Hamidreza Ghorbani, and Jose Luis Romeral Martinez. A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory. *IEEE Transactions on Industrial Electronics*, 64(11):9032–9042, 2017.

[13] Andrew N. Lemmon, Robert Cuzner, James Gafford, Rasoul Hosseini, Aaron D. Brovont, and Michael S. Mazzola. Methodology for characterization of common-mode conducted electromagnetic emissions in wide-bandgap converters for ungrounded shipboard applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6(1):300–314, 2018.

[14] Robin Getz and Bob Moeckel. Understanding and eliminating EMI in Microcontroller Applications, AN1050. 1996.

[15] Lu Wang, Yanjun Shi, and Hui Li. Anti-EMI Noise Digital Filter Design for a 60-kW Five-Level SiC Inverter Without Fiber Isolation. *IEEE Transactions on Power Electronics*, 33(1):13–17, 2018.

[16] Henry W. Ott. Noise Reduction Techniques in Electronic Systems, 1988.

[17] Pithadia Sanjay and Shridhar More. Texas Instruments: Grounding in mixed-signal systems demystified , Part 1. *Analog Applications Journal*, (2Q):5–8, 2013.

[18] Sanjay Pithadia and Shridhar More. Grounding in mixed-signal systems demystified, Part 2. *Analog Applications Journal*, (2Q):5–8, 2013.

[19] Alexander Weiler, Alexander Pakosta, and Ankur Verma. High-Speed Layout Guidelines Application Report High-Speed Layout Guidelines. (November 2006):1–21, 2017.

[20] Texas Instruments. High-Speed Interface Layout Guidelines. (August 2014):1–23, 2015.

[21] David Reusch and Johan Strydom. Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter. *IEEE Transactions on Power Electronics*, 29(4):2008–2015, 2014.

[22] Intel. Board Design Resource Center. https://www.intel.com/content/www/us/en/programmable resources/support-centers/board-design-guidelines.html.

[23] James Palmer, Shiqi Ji, William Giewont, Fei Fred Wang, and Leon M Tolbert. Improving Voltage Sensor Noise Immunity in a High Voltage and High dv / dt Environment. pages 107–113, 2020.

[24] Jianghui Yu, Rolando Burgos, and Dushan Boroyevich. EMI Study on Control Implementation in PEBB-based Converter. *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics, COMPEL 2018*, pages 1–5, 2018.

[25] Shanthi Pavan, Richard Schreier, and Gabor C Temes. DELTA-SIGMA DATA CONVERTERS.

[26] Steven R Norsworthy, Richard Schreier, and Gabor C Temes. Steven R. Norsworthy, Richard Schreier, Gabor C. Temes-Delta-Sigma Data Converters_ Theory, Design, and Simulation, 1997.

[27] Jan Gottschlich, Pelle Weiler, Markus Neubert, and Rik W. De Doncker. Delta-sigma modulated voltage and current measurement for medium-voltage DC applications. *2017 19th European Conference on Power Electronics and Applications, EPE 2017 ECCE Europe*, 2017-Janua:1–9, 2017.

[28] Texas Instruments Inc. Temperature sensing with NTC circuit. *Analog Engineer's Circuit: Amplifiers*, (December):1–5, 2018.

[29] Multirate Digital Filters, Filter Banks, and Polyphase Networks. Multirate Digital Filters, Filter Banks, Polyphase Networks,. 78(1), 1990.

[30] Ljiljana Milić, Tapio Saramäki, and Robert Bregović. Multirate filters: An overview. *IEEE Asia-Pacific Conference on Circuits and Systems, Proceedings, APCCAS*, 00:912–915, 2006.

[31] R. A. Valenzuela and A. G. Constantinides. Digital signal processing schemes for efficient interpolation and decimation. *IEE Proceedings G: Electronics Circuits and Systems*, 130(6):225–235, 1983.

[32] Sevket Cetinsel, Richard C.S. Morling, and Izzet Kale. An FPGA based decimation filter processor design for real-time continuous-time Σ-Δ Modulator performance measurement and evaluation. *2011 20th European Conference on Circuit Theory and Design, ECCTD 2011*, pages 397–400, 2011.

[33] Brian P. Brnadt and Bruce A. Wooley. Versatile, efficient digital filter for decimation and interpolation. *1993 Symposium on VLSI Circuits Digest of Technical Papers*, pages 79–80, 1993.

[34] Eugene B. Hogenauer. An Economical Class of Digital Filters for Decimation and Interpolation. *IEEE Transactions on Acoustics, Speech, and Signal Processing*, 29(2):155–162, 1981.

[35] Zhaochun Lu, Xiaohong Peng, Wuchen Wu, Ligang Hou, and Yong He. Design of 16 bit digital filter used in Delta-Sigma A/D converter. *ICCET 2010 - 2010 International Conference on Computer Engineering and Technology, Proceedings*, 4(1):484–487, 2010.

[36] S. Boujelben, C. H. Rebai, D. Dallet, and P. H. Marchegay. Design simulation of decimation filter for sigma delta converters. *11th IMEKO TC4 Symposium on Trends in Electrical Measurements and Instrumentation and 6th IMEKO TC4 Workshop on ADC Modelling and Testing 2001*, pages 594–598, 2001.

[37] Brian Pisani. Digital Filter Types in Delta-Sigma ADCs. (May):1–8, 2017.

[38] Miroslav Oljaca and Tom Hendrick. Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications. *Texas Instruments*, (June):1–22, 2003.

[39] MathWorks. Implementing the Filter Chain of a Digital Down-Converter in HDL - MATLAB & Simulink - MathWorks Deutschland. https://de.mathworks.com/help/dsp/ug/implementing-the-filter-chain-of-a-digital-down-converter-in-hdl.html.

[40] MathWorks. HDL Implementation of a Digital Down-Converter for LTE - MATLAB & Simulink - MathWorks Deutschland. https://de.mathworks.com/help/dsp/ug/hdl-implementation-of-digital-down-converter-for-LTE.html.

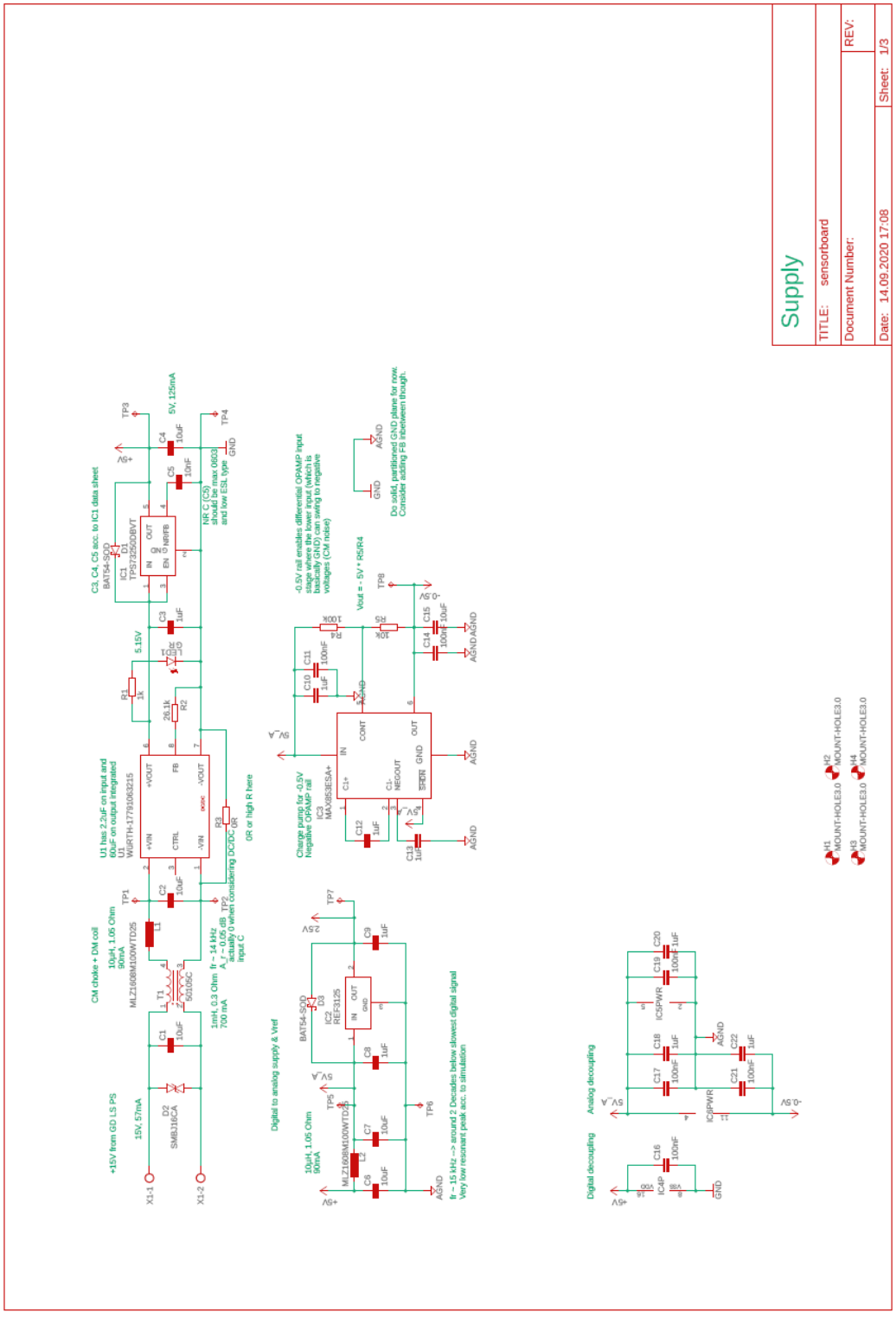
[41] MathWorks. Design of Decimators/Interpolators - MATLAB & Simulink - MathWorks Deutschland. https://de.mathworks.com/help/dsp/ug/design-of-decimators-interpolators.html.

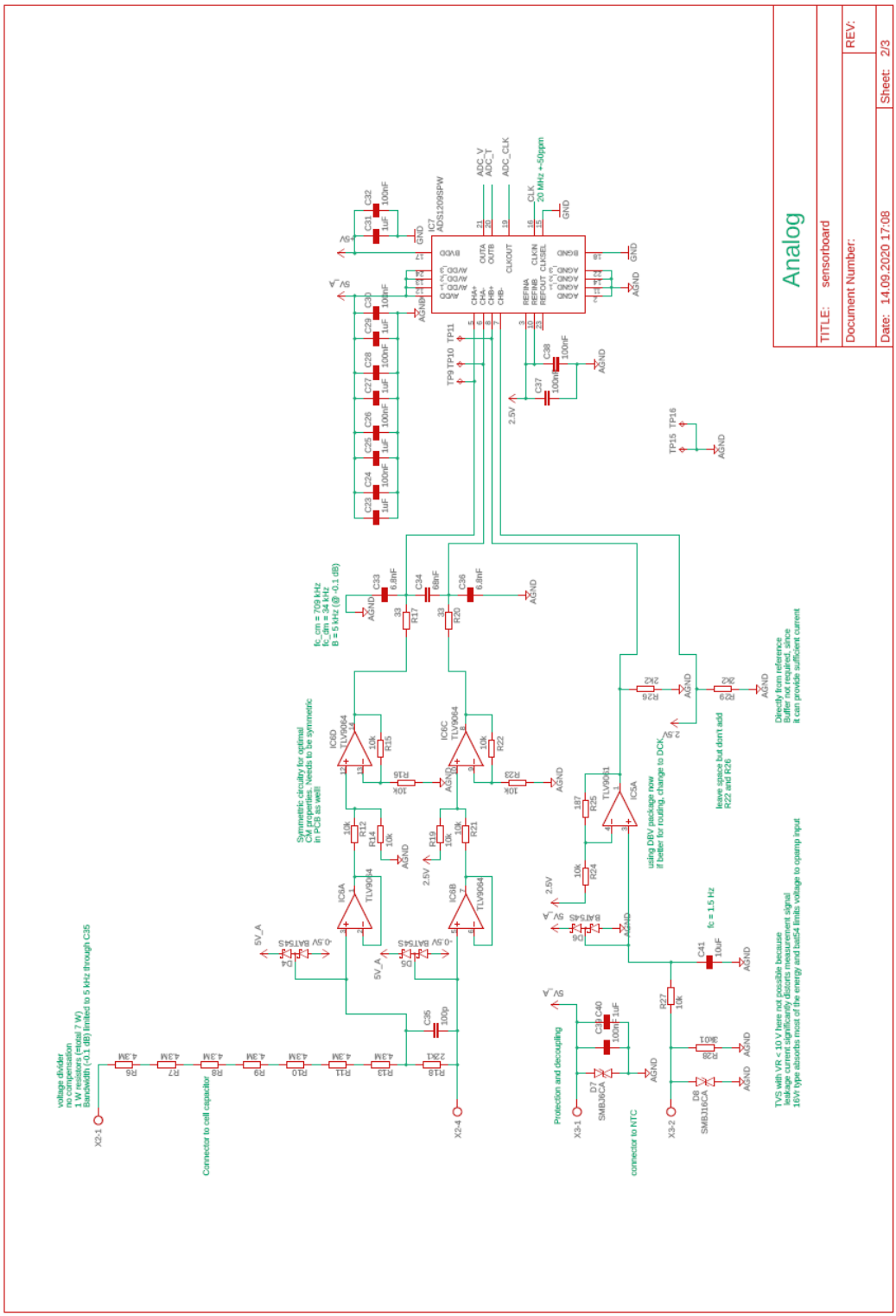
[42] MathWorks. Multistage Design Of Decimators/Interpolators - MATLAB & Simulink - MathWorks Deutschland. https://de.mathworks.com/help/dsp/ug/multistage-design-of-decimators-interpolators.html;jsessionid=08763f4672367b164c88e0bbda25.

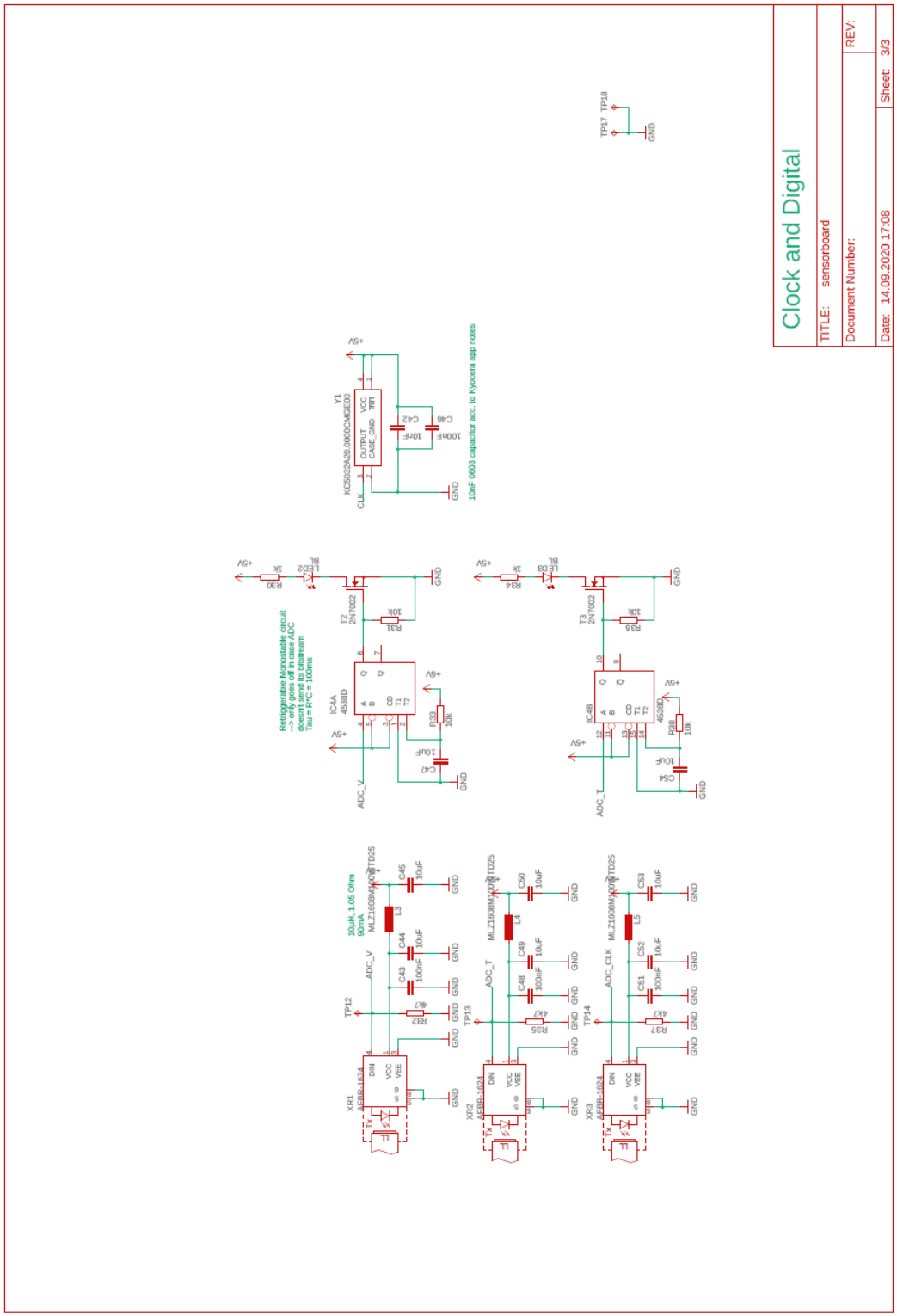
[43] MathWorks. Designing Low Pass FIR Filters - MATLAB & Simulink - MathWorks Deutschland. https://de.mathworks.com/help/dsp/ug/designing-low-pass-fir-filters.html.

11 Appendix

11.1 Sensor board circuit

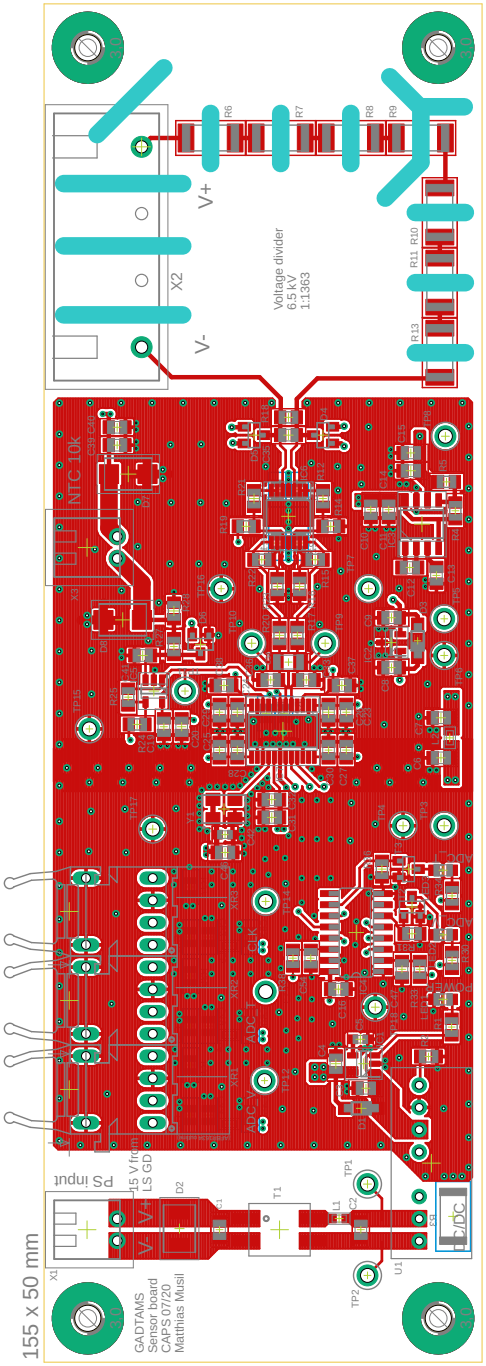



Analog
TITLE: sensorboard
Document Number:
REV:
Date: 14.09.2020 17:08
Sheet: 2/3
IC7 ADS1209SPW
ADC_V
ADC_T
ADC_CLK
CLK 20 MHz +-50ppm
IC6D TLV9064
IC6C TLV9064
IC6A TLV9061
IC6B TLV9064
fc_sin = 709 kHz
fc_min = 3,4 kHz
B = 5 kHz (@ -0,1 dB)
Symmetric circuitry for optimal CM properties. Needs to be symmetric in PCB iss well
leave space but don't add R22 and R26
using DBV package now if better for routing, change to DCK
Directly from reference Buffer not needed as it can provide sufficient current
fc = 1,5 Hz
voltage divider no compensation 1 W resistors (=total 7 W) Bandwidth (-0,1 dB) limited to 5 kHz through C35
Connector to cell capacitor
connector to NTC
Protection and decoupling
TVS with VR < 10 V here not possible because leakage current < 1 µA which would distort measurement signal 16V type absorbs most of the energy and batEx limits voltage to opamp input
D7 SMBJ6CA
D8 SMBJ16CA
BAT54S
AGND
GND
2,5V
5V_A
X2-1
X2-4
X3-1
X3-2

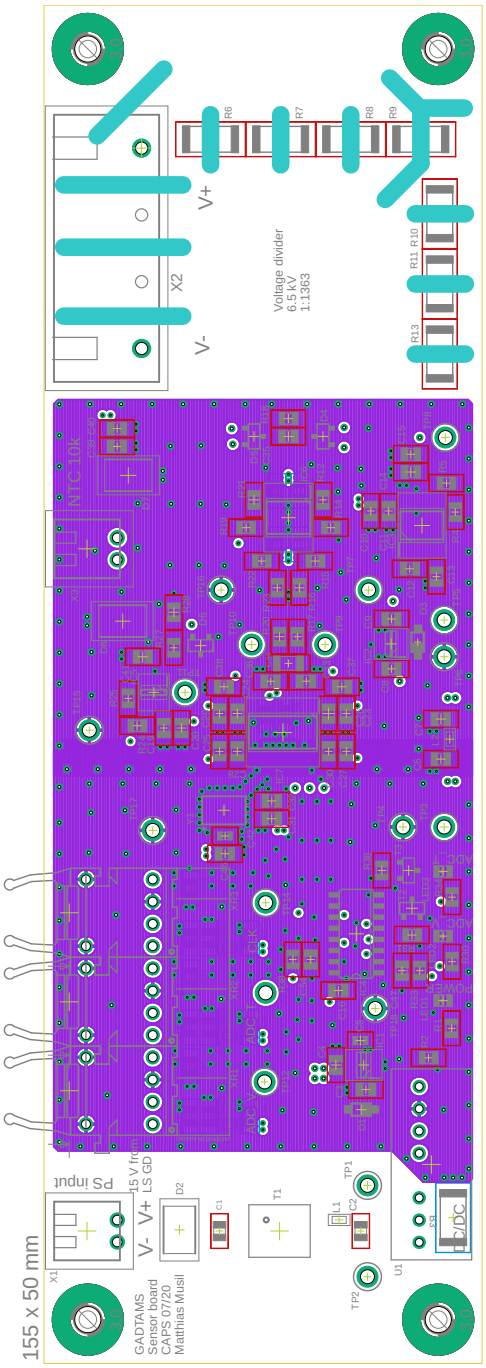

Clock and Digital
TITLE: sensorboard
Document Number:
REV:
Date: 14.09.2020 17:08
Sheet: 3/3
10nF 0603 capacitor acc. to Kyocera app notes
Retriggerable Monostable circuit
--> only goes off in case ADC
doesn't send a signal
Tau = R*C = 100ns
10µH, 1.05 Ohm
0603_1

11.2 Sensor board PCB layers

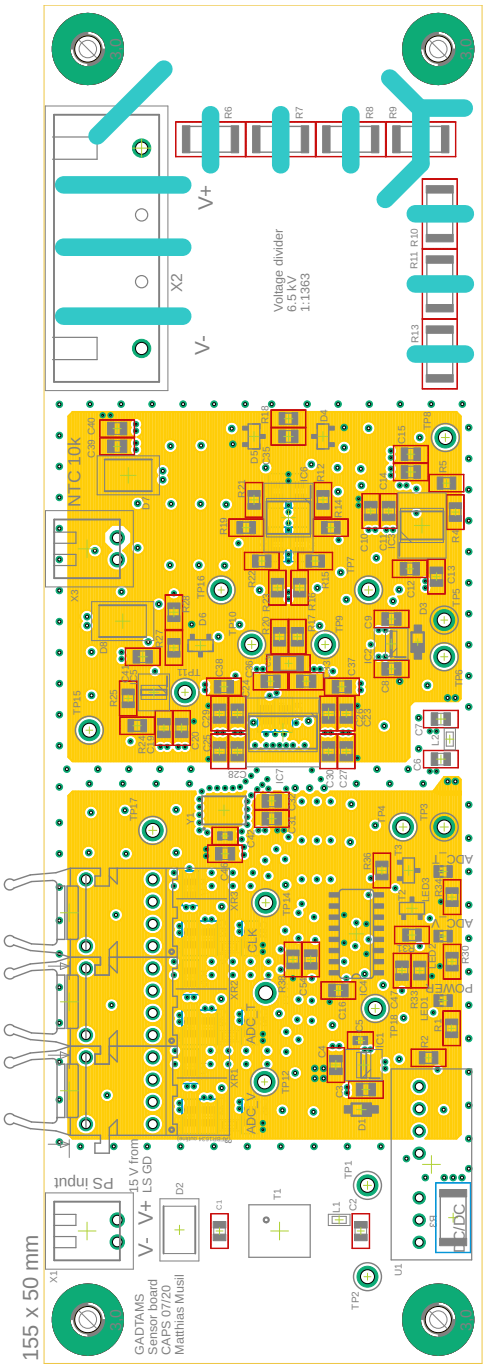
11.2.1 Layer 1



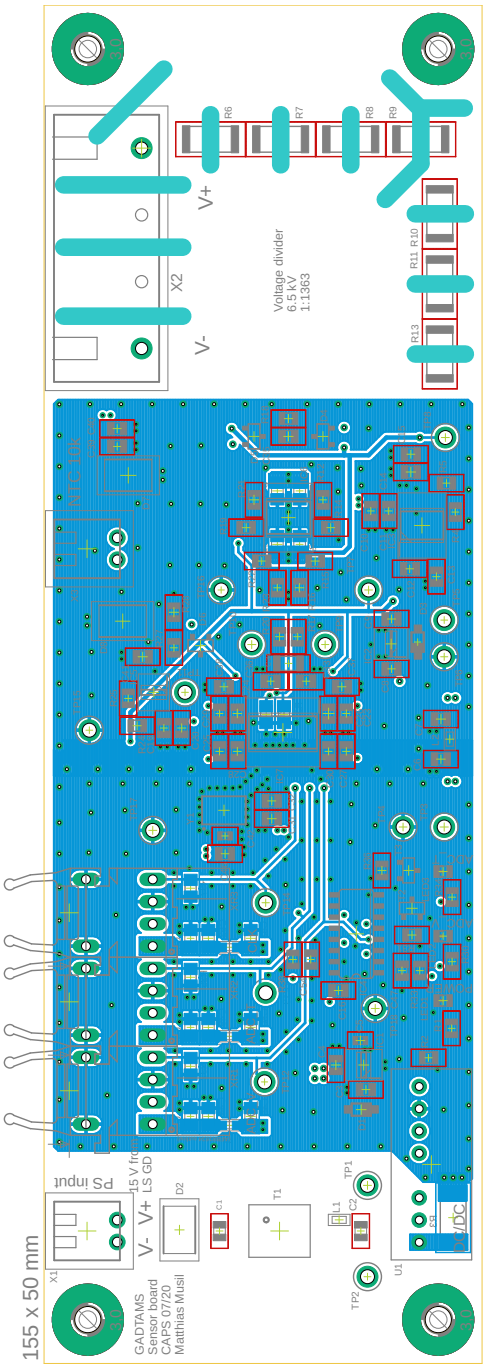
11.2.2 Layer 2


V+
V-
X2
R6
R7
R8
R9
R10
R11
R13
Voltage divider
6.5 kV
1:1363
155 x 50 mm
GADTAMS
Sensor board
CAPS 07/20
Matthias Musil
V- V+ LS GD
15 V fro
PS Input
D2
C1
T1
TP1
TP2
L1
C2
U1
D3
DC/DC

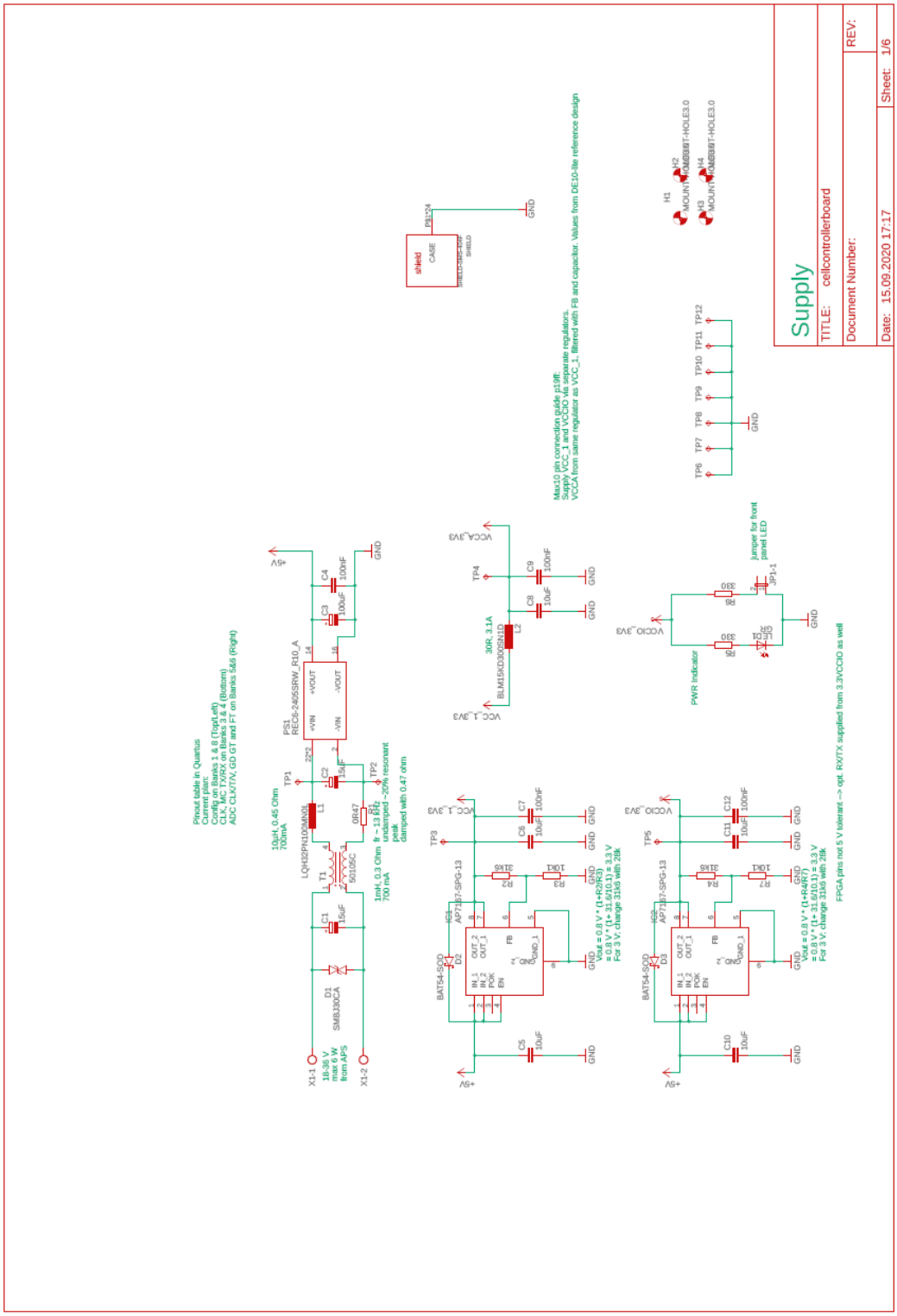
11.2.3 Layer 3

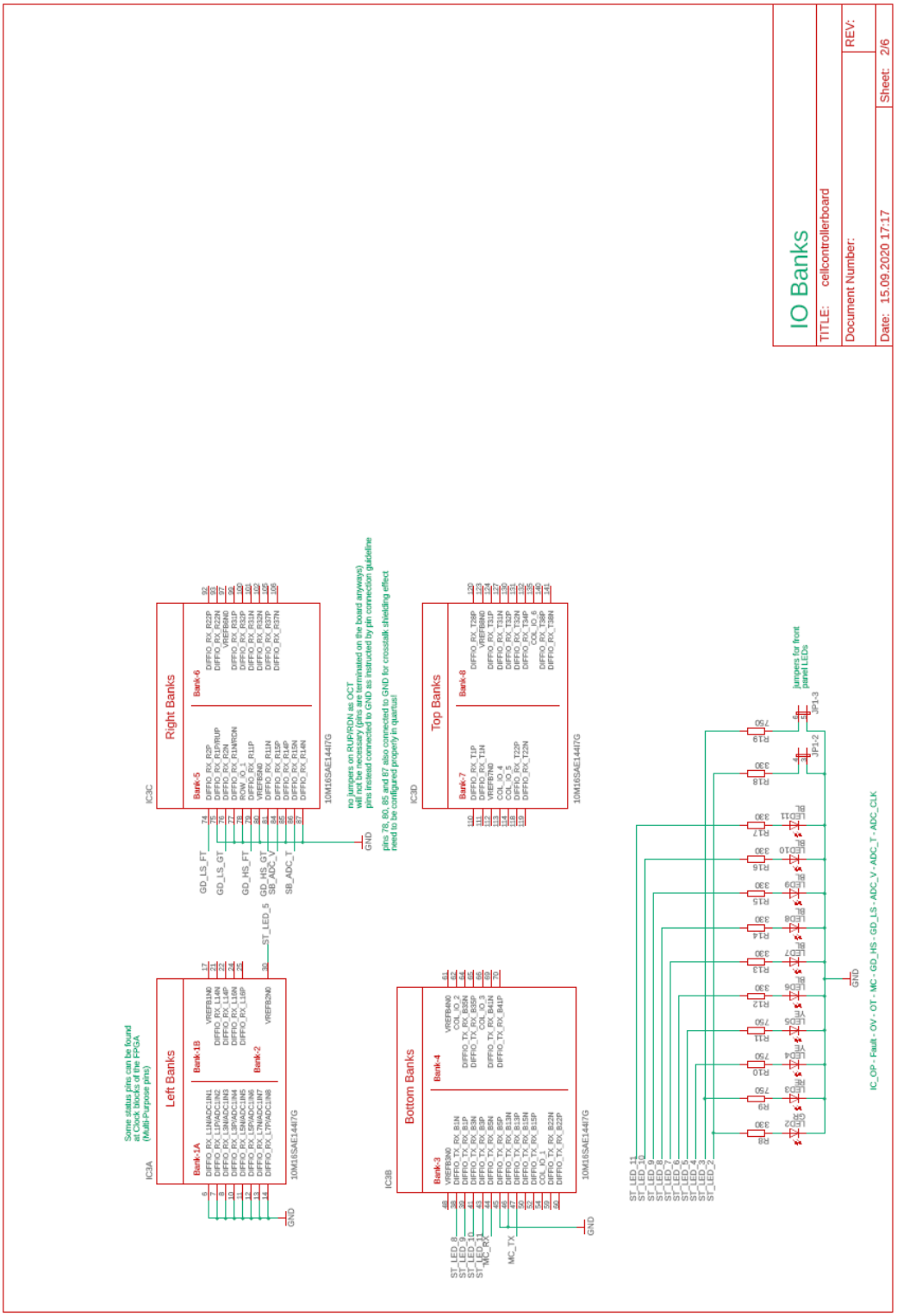

V+
V-
X2
Voltage divider
6.5 kV
1:1363
R6
R7
R8
R9
R10
R11
R13
NTC 10K
PS Input
15 V from LS GD
V- V+
155 x 50 mm
GADTAMS
Sensor board
CAPS 07/20
Matthias Musil

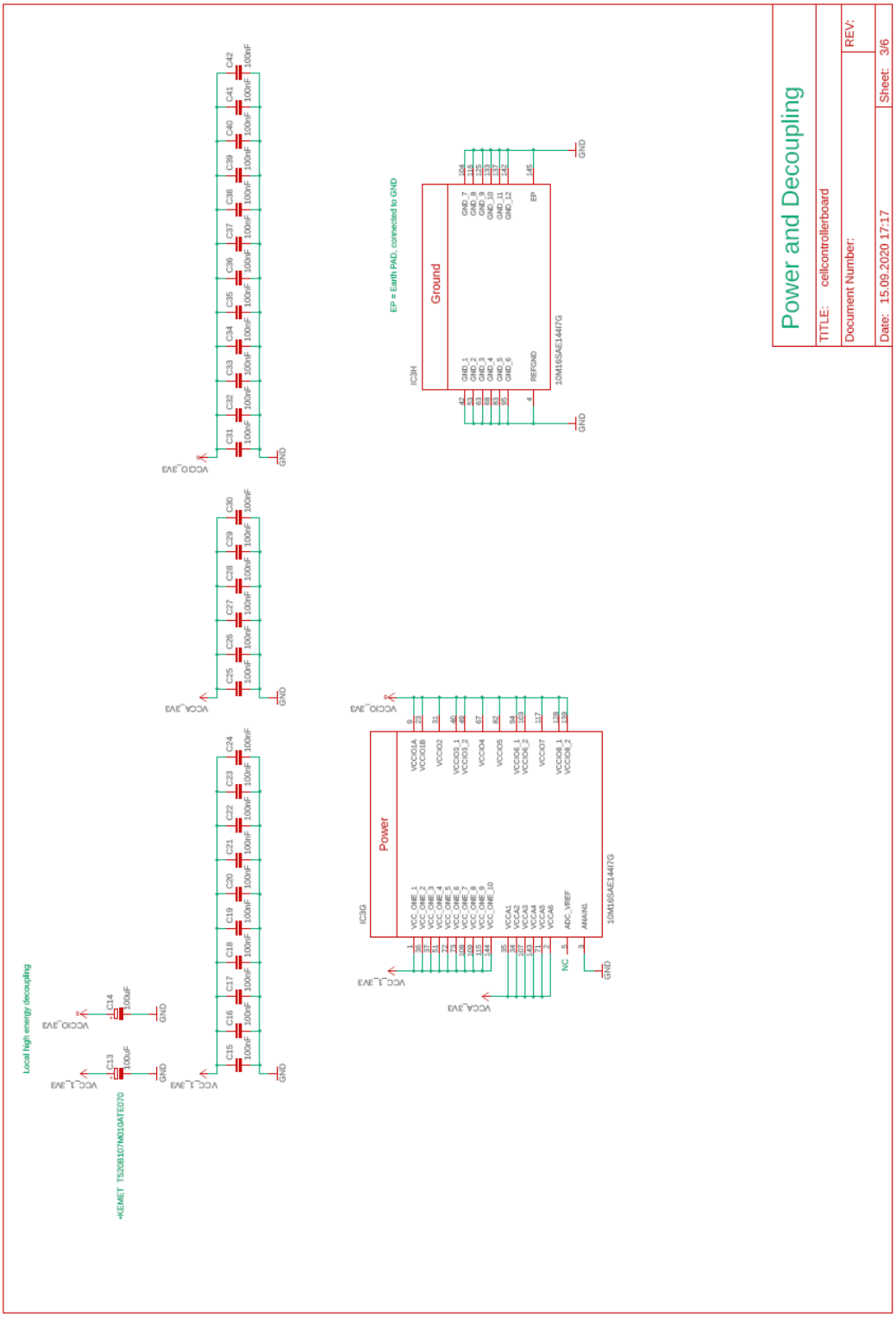
11.2.4 Layer 4

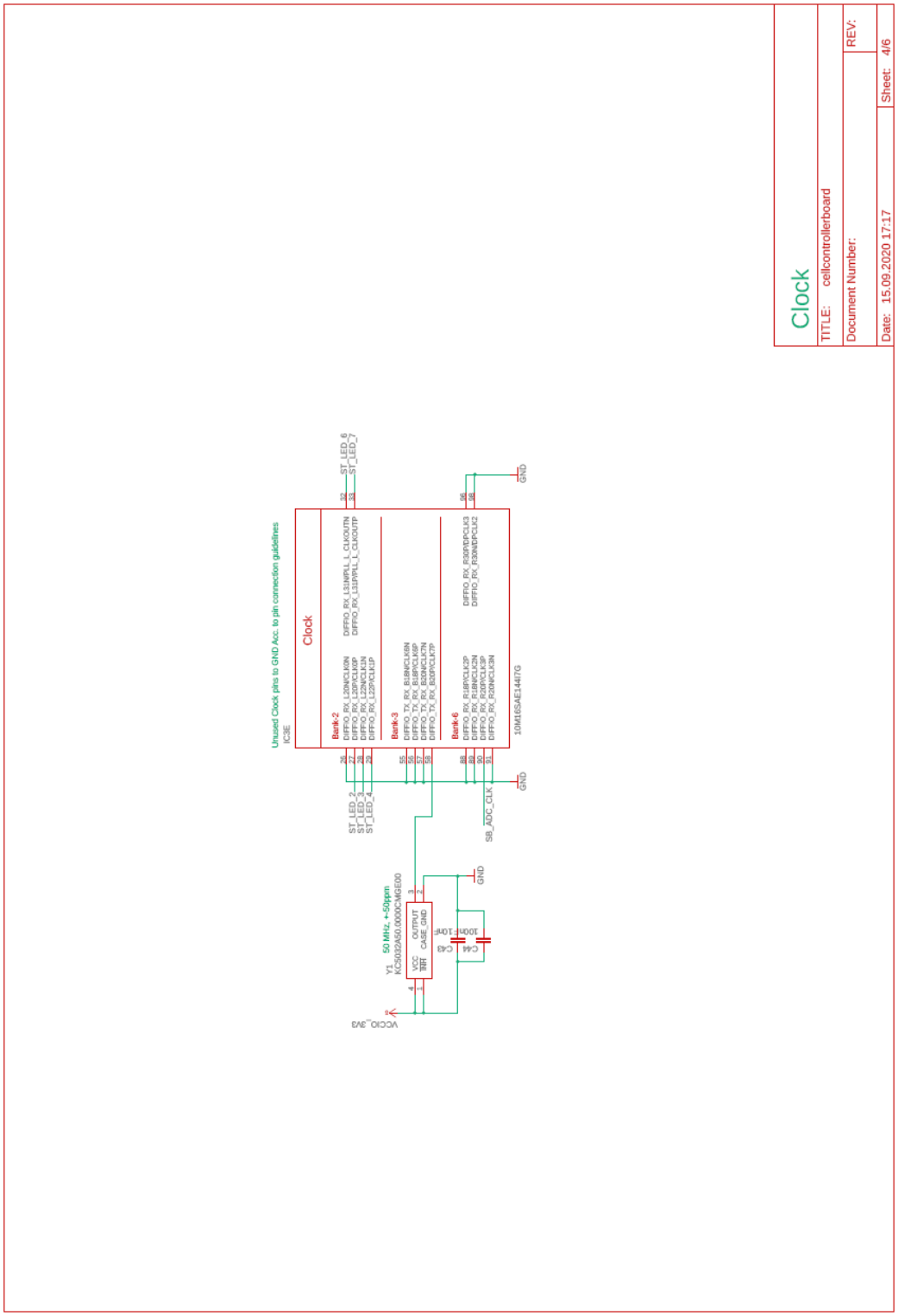

V+
V-
X2
Voltage divider
6.5 kV
1:1363
R6
R7
R8
R9
R10
R11
R13
155 x 50 mm
GADTAMS
Sensor board
CAPS 07/20
Matthias Musil
V- V+ LS GD
PS Input
TP1
TP2
T1
D2
U1

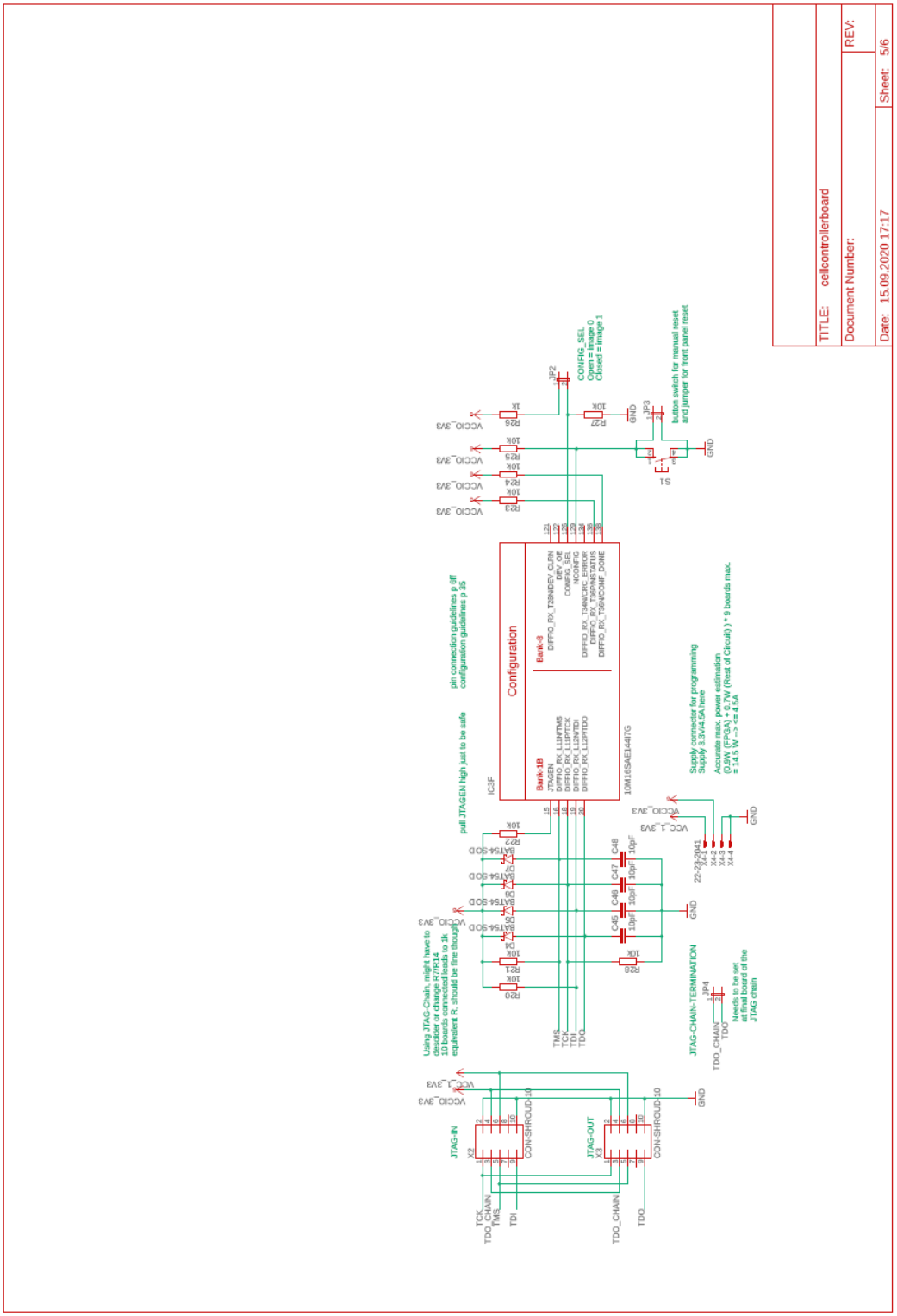
11.3 Cell controller board circuit

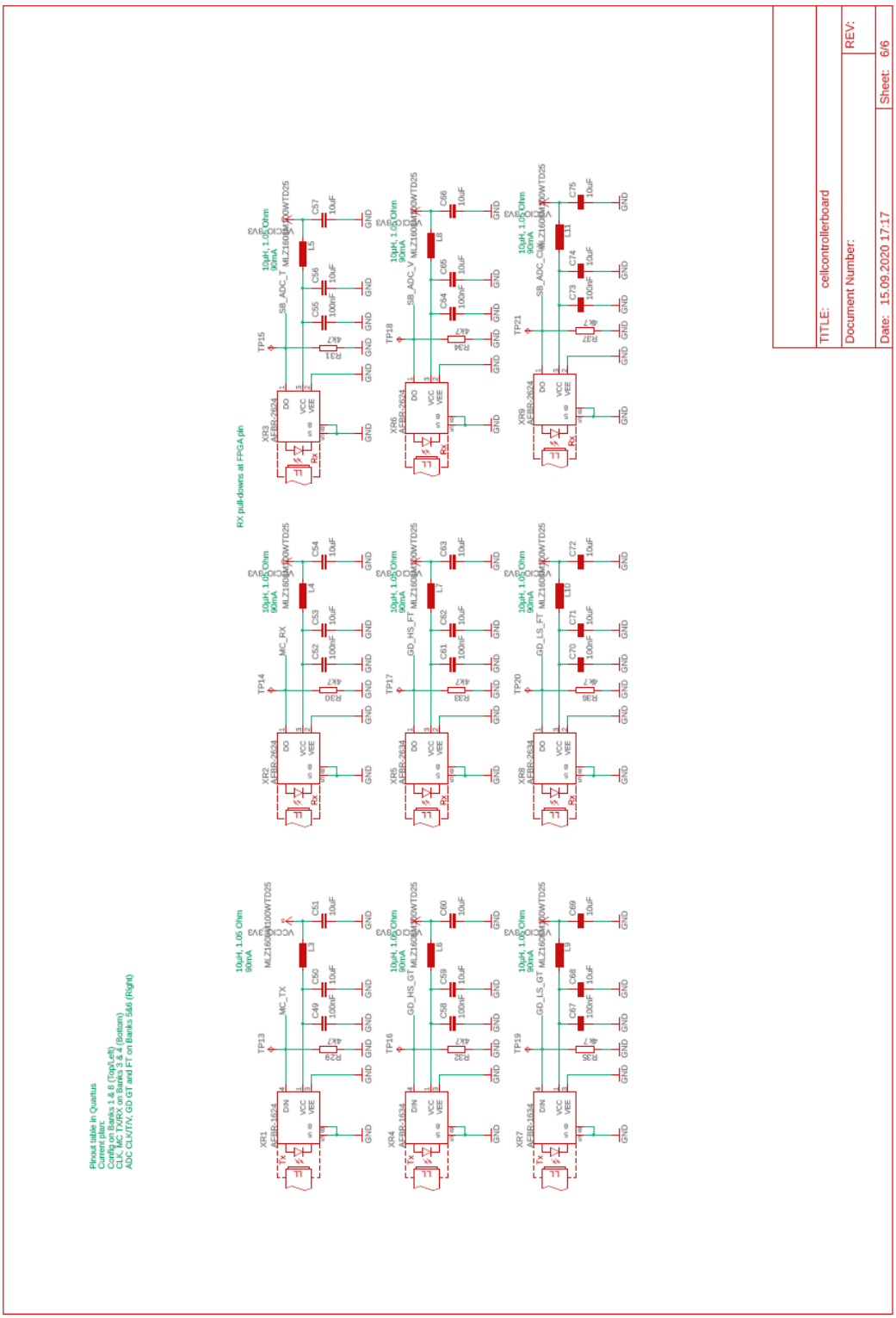



IO Banks
TITLE: cellcontrollerboard
Document Number:
REV:
Date: 15.09.2020 17:17
Sheet: 2/6
Right Banks
Left Banks
Top Banks
Bottom Banks
10M16SAE144I7G
no jumpers on RUP/RDN as OCT
will not be necessary (pins are terminated on the board anyways)
pins instead connected to GND as instructed by pin connection guideline
pins 78, 80, 85 and 87 also connected to GND for crosstalk shielding effect
need to be configured properly in quartus!
Some status pins can be found at Clock blocks of the FPGA (Multi-Purpose pins)
Jumpers for front panel LEDs
IC_OP - Fault - OV - OT - MC - GD_HS - GD_LS - ADC_V - ADC_T - ADC_CLK
GND


Power and Decoupling
TITLE: cellcontrollerboard
Document Number:
REV:
Date: 15.09.2020 17:17
Sheet: 3/6
Ground
Power
EP = Earth PAD, connected to GND
Local high energy decoupling
10M16SAE144I7G
VCCIO_3V3
VCCA_3V3
VCC_L_3V3
GND

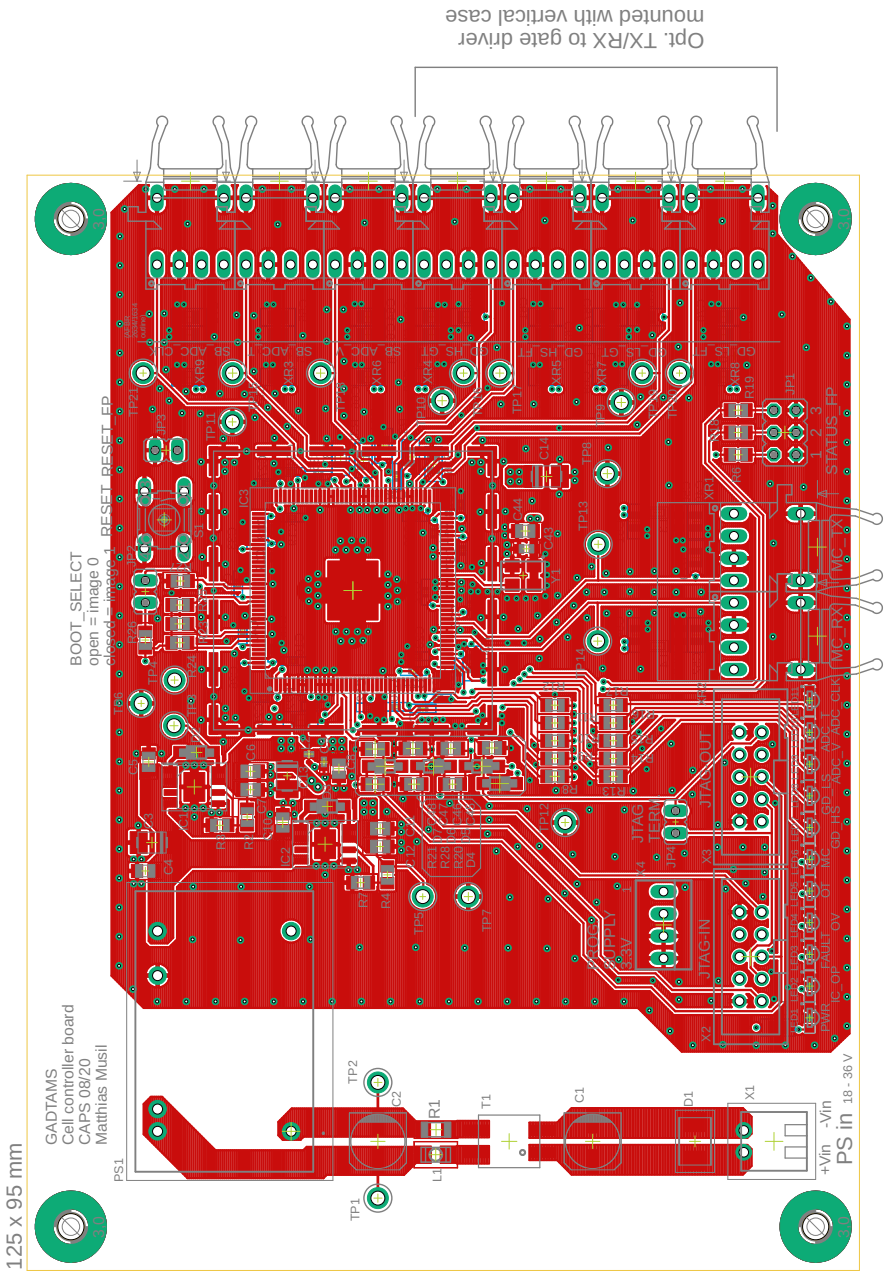

Clock
TITLE: cellcontrollerboard
Document Number:
REV:
Date: 15.09.2020 17:17
Sheet: 4/6
Unused Clock pins to GND Acc. to pin connection guidelines
IC3E
Clock
Bank-2
Bank-3
Bank-6
10M16SAE144I7G
ST_LED_6
ST_LED_7
ST_LED_2
ST_LED_3
ST_LED_4
SB_ADC_CLK
GND
VCCIO_3V3
50 MHz +-50ppm
OUTPUT
CASE_GND
VCC
C43
C44
100nF
10nF


TITLE: cellcontrollerboard
Document Number:
REV:
Date: 15.09.2020 17:17
Sheet: 5/6
Configuration
JTAG-IN
JTAG-OUT
JTAG-CHAIN-TERMINATION
CON-SHROUD10
button switch for manual reset and jumper for front panel reset
pull JTAGEN high just to be safe
pin connection guidelines p 35
configuration guidelines p 35
Supply connector for programming
Supply 3.3V/4.5A here
Accurate max. power estimation
(0.5W (FPGA) + 0.7W (Rest of Circuit)) * 9 boards max.
≈ 14.5 W --> < 4.5A
Needs to be set at final board of the JTAG chain
Using JTAG-Chain, might have to desolder or change R7764 10 boards connected: Has to 1k equivalent R, should be fine though

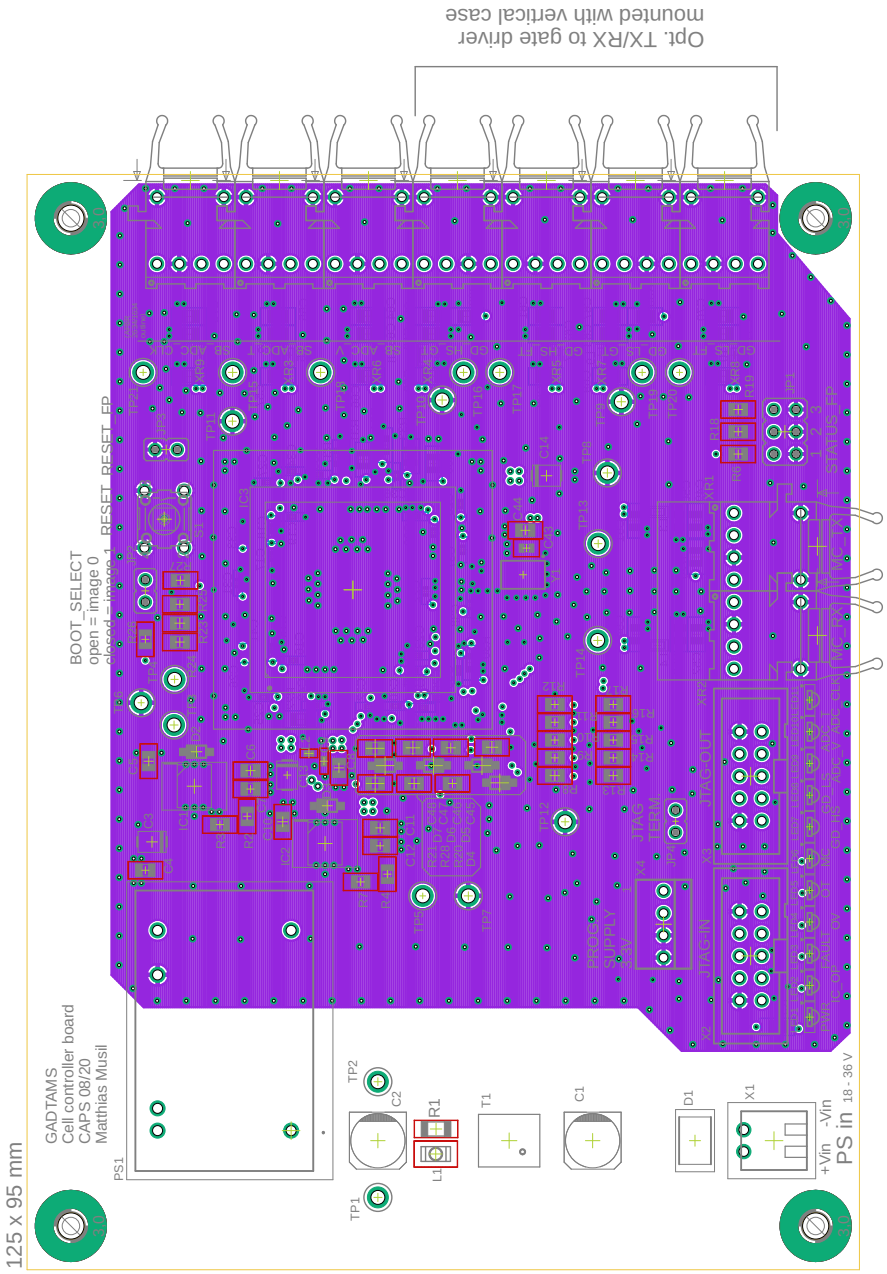

TITLE: cellcontrollerboard
Document Number:
REV:
Date: 15.09.2020 17:17
Sheet: 6/6
Pinout table in Quartus
Current plan:
Config on Banks 1 & 8 (Top/Left)
CLK_FC_TX/RX on Banks 3 & 4 (Bottom)
ADC CLK/TV, GD GT and FT on Banks 5&6 (Right)
RX pull-downs at FPGA pin
SB_ADC_T
SB_ADC_V
SB_ADC_CM
MC_RX
GD_HS_FT
GD_LS_FT
MC_TX
GD_HS_GT
GD_LS_GT
10µH, 1.05 Ohm
90mA
MLZ1608M100WTD25
AEBR-2624
AEBR-1624
10uF
100nF
4K7

11.4 Cell controller board PCB layers

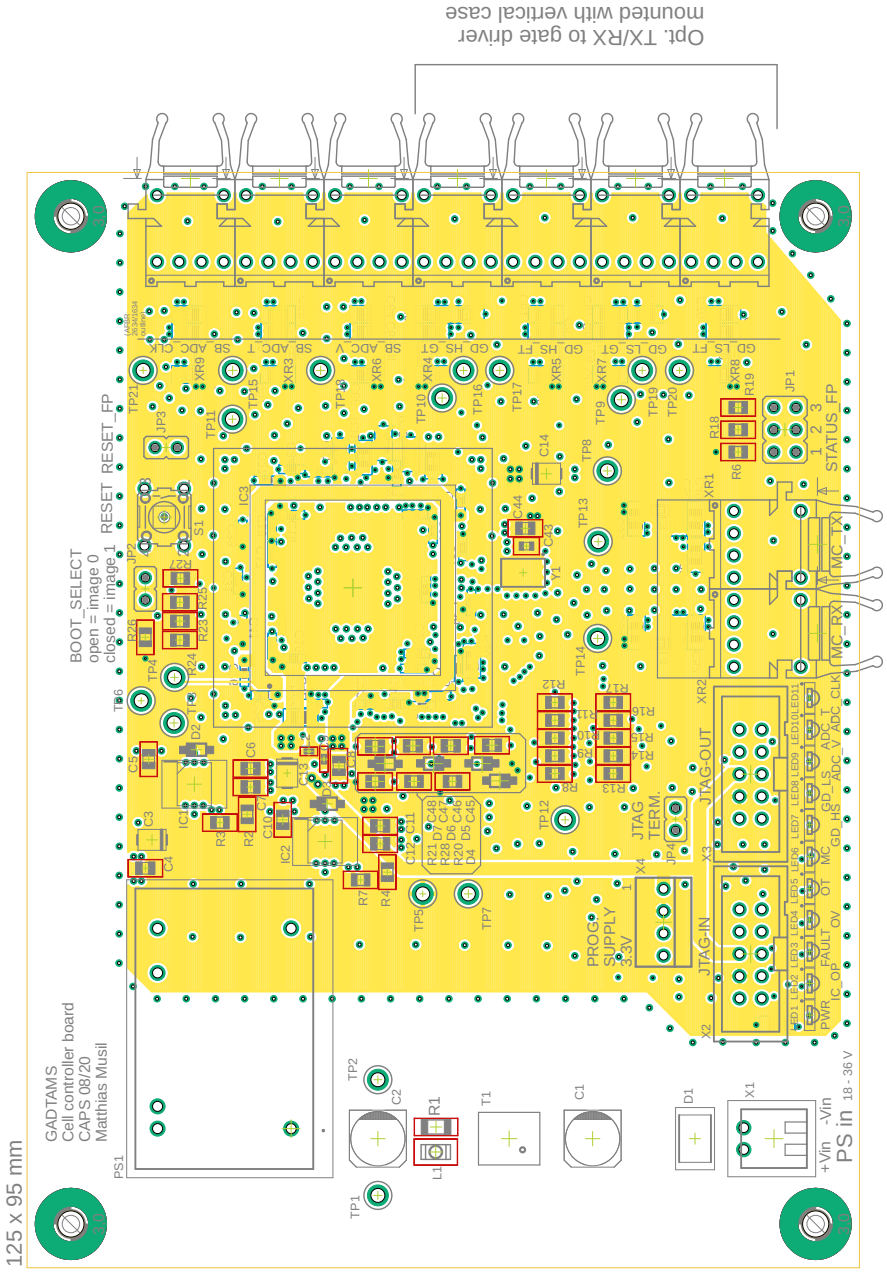
11.4.1 Layer 1



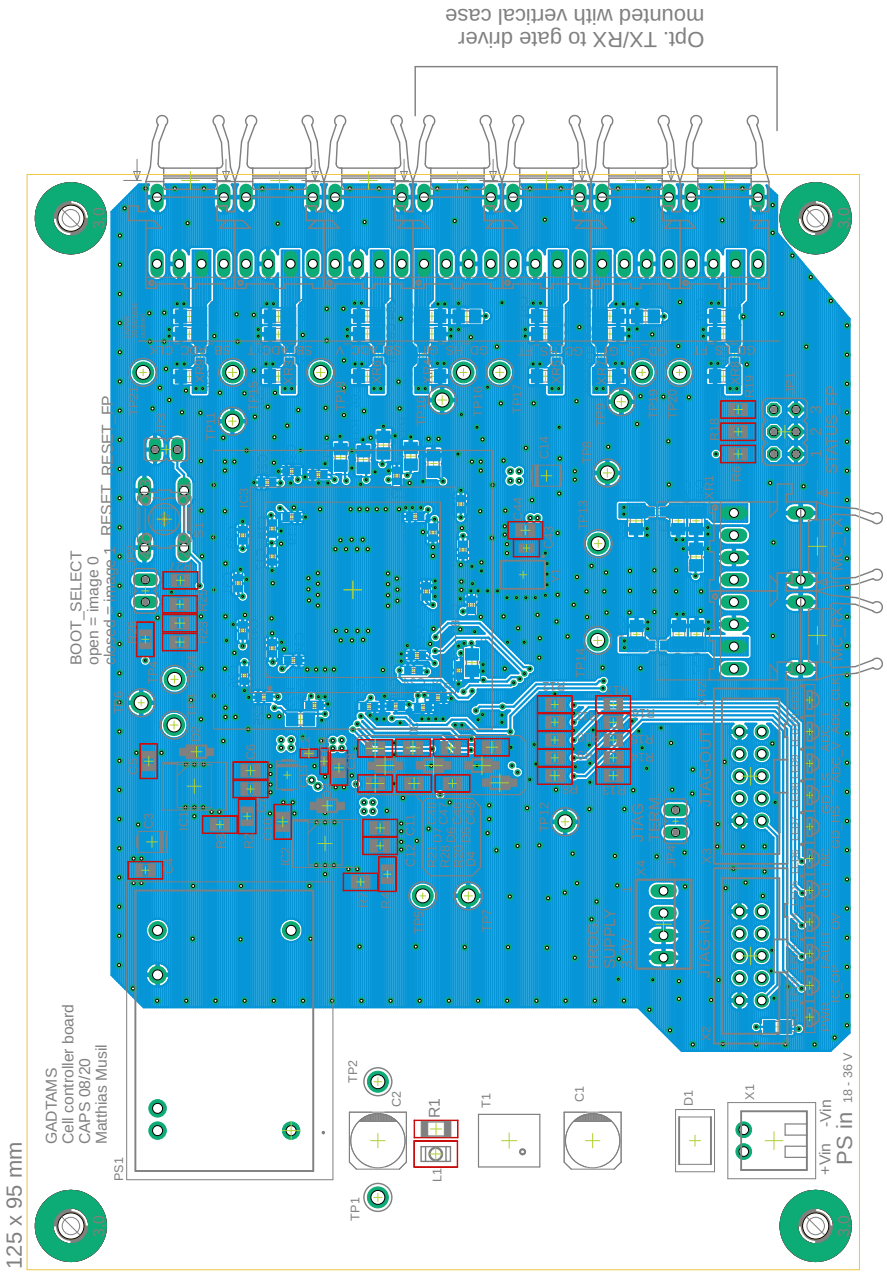
11.4.2 Layer 2


Opt. TX/RX to gate driver
mounted with vertical case
BOOT_SELECT
open = image 0
closed = image 1
RESET_RESET_FP
GADTAMS
Cell controller board
CAPS 08/20
Matthias Musil
125 x 95 mm
PS in 18 - 36 V
+Vin -Vin
PS1
TP1
TP2
C2
R1
L1
T1
C1
D1
X1

11.4.3 Layer 3


Opt. TX/RX to gate driver
mounted with vertical case
GADTAMS
Cell controller board
CAPS 08/20
Matthias Musil
125 x 95 mm
PS in 18 - 36 V
+Vin -Vin
BOOT_SELECT
open = image 0
closed = image 1
RESET
RESET_FP
STATUS_FP
JTAG-OUT
JTAG-IN
JTAG TERM.
PROG SUPPLY 3.3V
MC_TX
MC_RX
ADC_CLK
ADC_V
ADC_I
GD_LS
GD_HS
MC_OT
FAULT
OV
IC_OT
PWR

11.4.4 Layer 4


Opt. TX/RX to gate driver
mounted with vertical case
BOOT_SELECT
open = image 0
closed = image 1
RESET
RESET_FP
GADTAMS
Cell controller board
CAPS 08/20
Matthias Musil
125 x 95 mm
PS1
TP2
C2
R1
L1
T1
C1
D1
X1
TP1
+Vin
-Vin
PS in
18 - 36 V